

PJQ4476AP-AU

100V N-Channel Enhancement Mode MOSFET

Voltage

100 V

Current

35 A

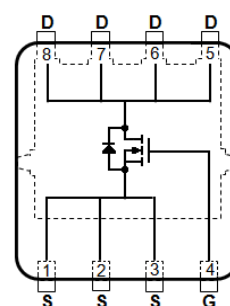
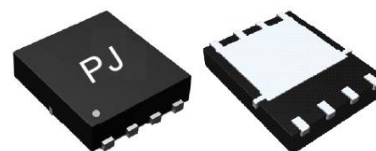
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@15A<25m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@10A<28.5m\Omega$
- High switching speed
- Improved dv/dt capability
- Low reverse transfer capacitance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.001 ounces, 0.03 grams

DFN3333-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (Note 4)	$T_C=25^{\circ}C$	I_D	35	A
	$T_C=100^{\circ}C$		22	
Pulsed Drain Current (Note 1)	$T_C=25^{\circ}C$	I_{DM}	140	
Power Dissipation	$T_C=25^{\circ}C$	P_D	62	W
	$T_C=100^{\circ}C$		25	
Continuous Drain Current (Note 4)	$T_A=25^{\circ}C$	I_D	6.3	A
	$T_A=70^{\circ}C$		5	
Power Dissipation	$T_A=25^{\circ}C$	P_D	2.0	W
	$T_A=70^{\circ}C$		1.3	
Single Pulse Avalanche Energy (Note 6)		E_{AS}	54	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^{\circ}C$
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	2	$^{\circ}C/W$
	Junction to Ambient	$R_{\theta JA}$	62.5	



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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

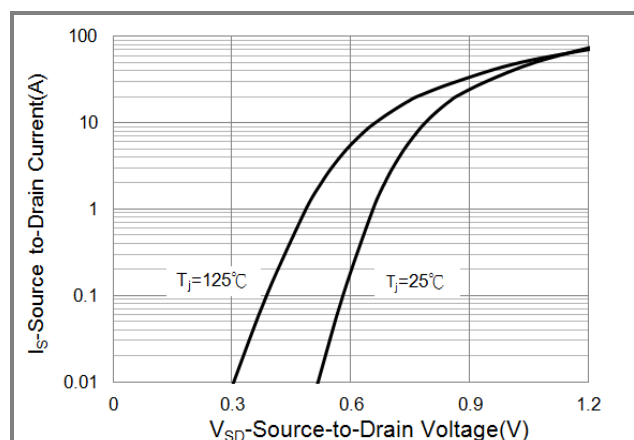
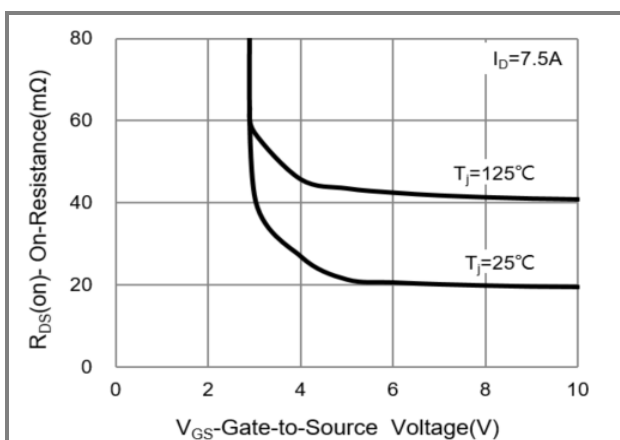
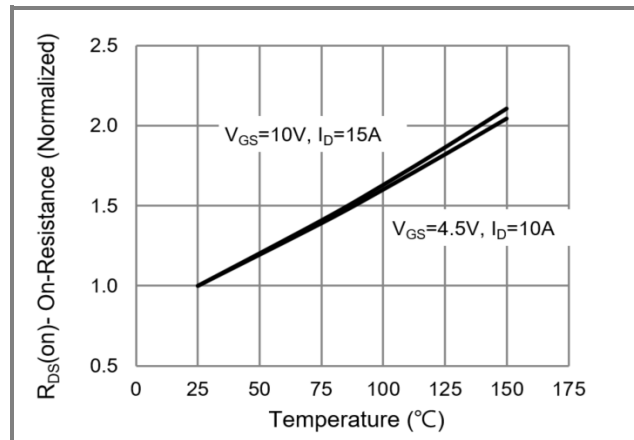
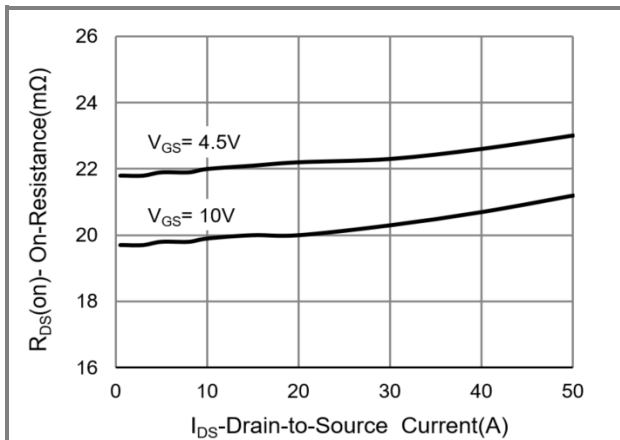
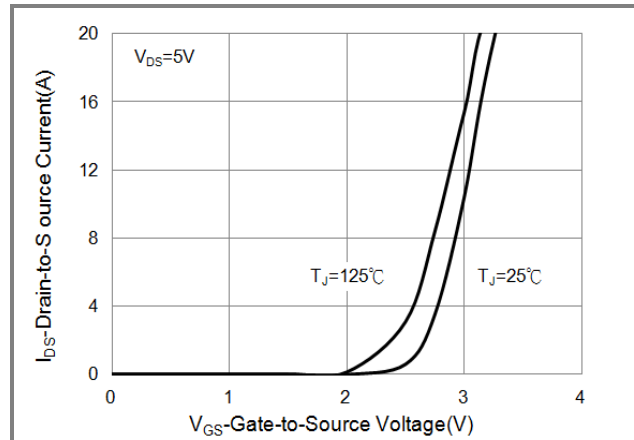
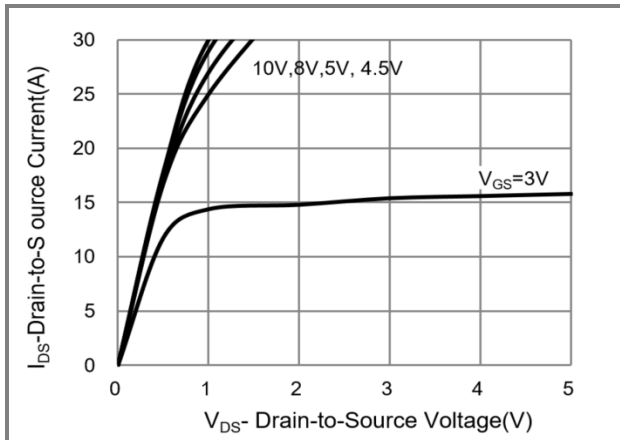
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	100	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	1.73	2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =15A	-	20	25	mΩ
		V _{GS} =4.5V, I _D =10A	-	22	28.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 5)						
Total Gate Charge	Q _g	V _{DS} =50V, I _D =10A, V _{GS} =10V (Note 2,3)	-	31	-	nC
Gate-Source Charge	Q _{gs}		-	5.1	-	
Gate-Drain Charge	Q _{gd}		-	7.3	-	
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHZ	-	1519	-	pF
Output Capacitance	C _{oss}		-	132	-	
Reverse Transfer Capacitance	C _{rss}		-	66	-	
Turn-On Delay Time	td _(on)	V _{DD} =50V, I _D =10A, V _{GS} =10V, R _G =3Ω (Note 2,3)	-	11	-	ns
Turn-On Rise Time	t _r		-	42	-	
Turn-Off Delay Time	td _(off)		-	40	-	
Turn-Off Fall Time	t _f		-	19	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	35	A
Reverse Recovery Time	V _{SD}	I _S =1A, V _{GS} =0V	-	0.68	1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
4. The maximum current rating is package limited.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. The test condition is $L=3\text{mH}$, $I_{AS}=6A$, $V_{DD}=50V$, $V_{GS}=10V$, Starting $T_J=25^{\circ}\text{C}$.
7. Guaranteed by design, not subject to production testing.

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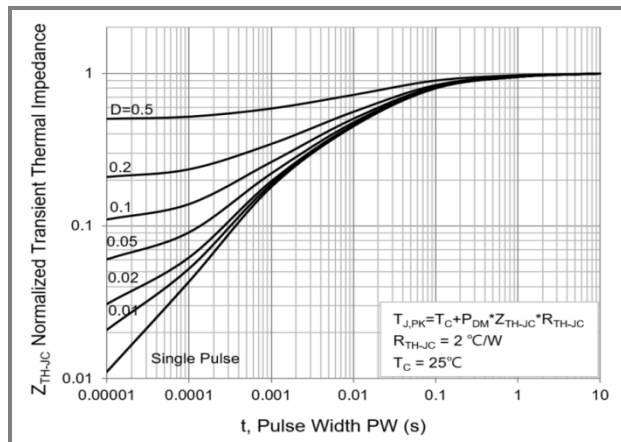
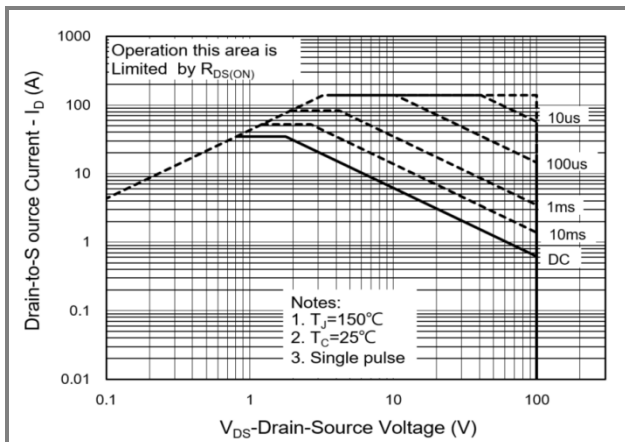
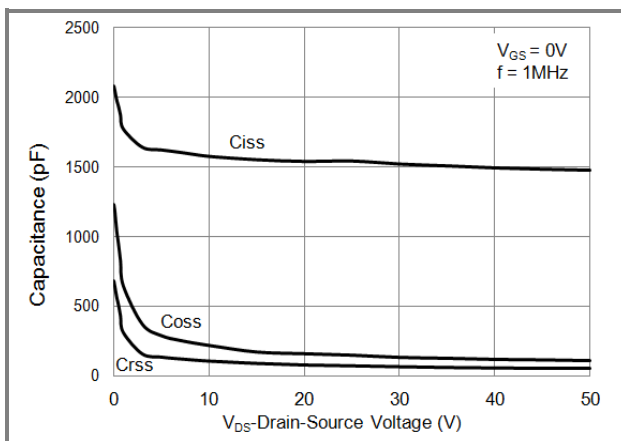
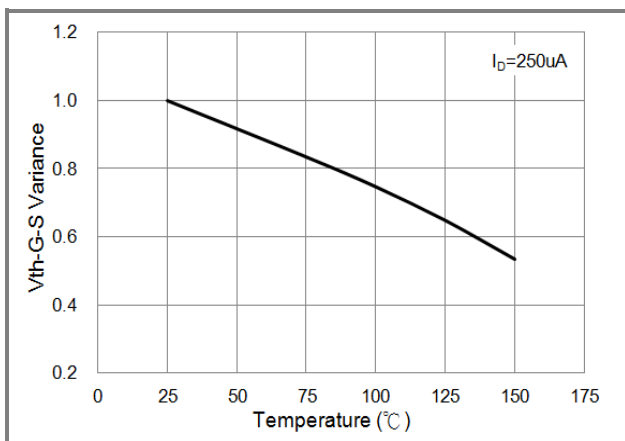
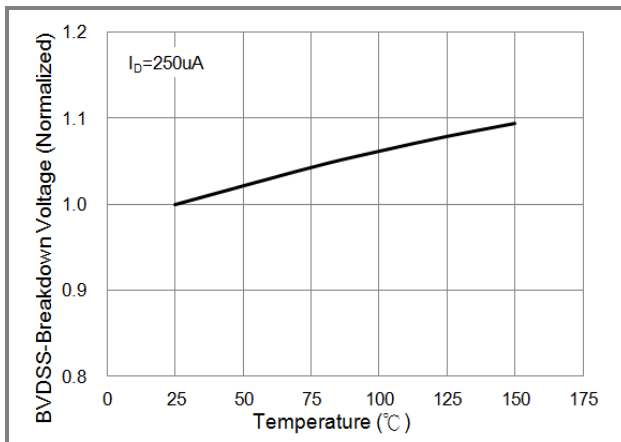
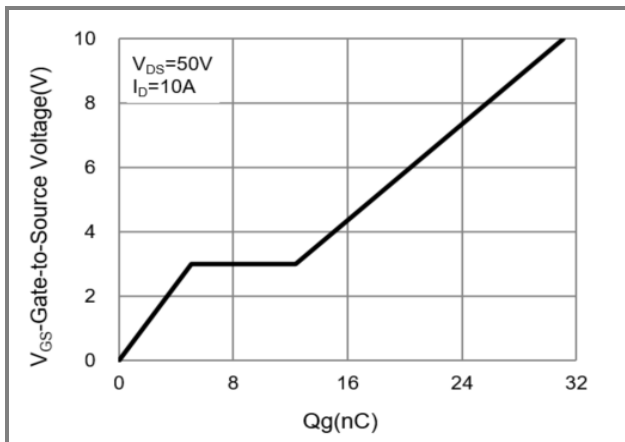
TYPICAL CHARACTERISTIC CURVES





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TYPICAL CHARACTERISTIC CURVES



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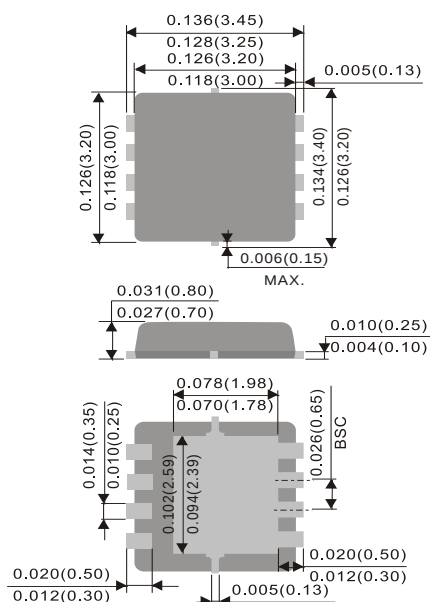
Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJQ4476AP-AU_R2_000A1	DFN3333-8L	5K pcs / 13" reel	4476	Halogen free

Packaging Information & Mounting Pad Layout

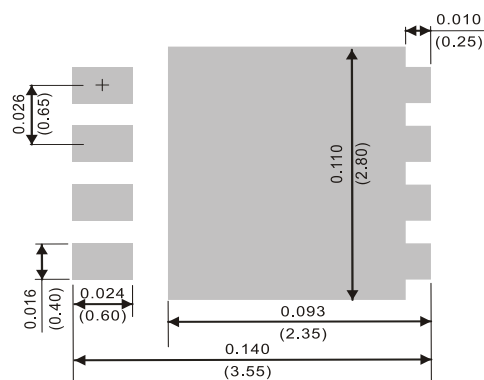
DFN3333-8L Dimension

Unit: inch(mm)



DFN3333-8L Pad Layout

Unit: inch(mm)





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