

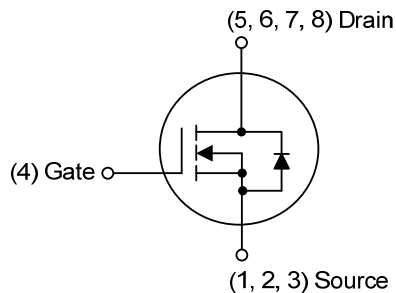
**UTT100N07****Power MOSFET****100A, 65V N-CHANNEL
POWER MOSFET****DESCRIPTION**

UTC **UTT100N07** is a N-Channel enhancement mode power field effect transistors are using trench DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

FEATURES

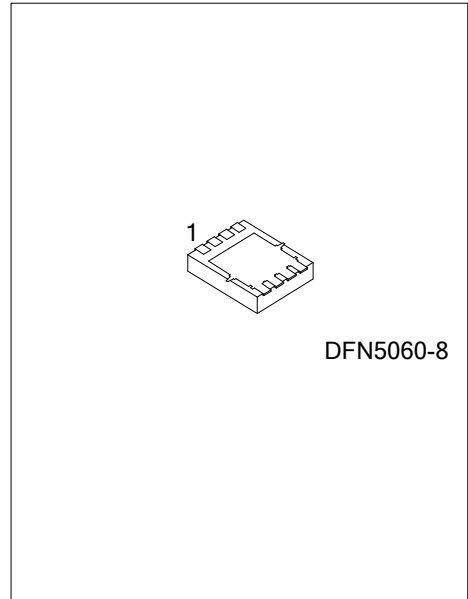
- * $R_{DS(ON)} \leq 2.8 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=20\text{A}$
 $R_{DS(ON)} \leq 5.4 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=10\text{A}$
- * Improved dv/dt capability
- * Fast switching
- * 100% EAS Guaranteed

SYMBOL**ORDERING INFORMATION**

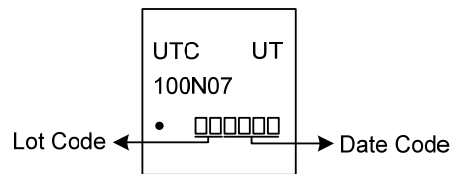
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT100N07L-K08-5060-R	UTT100N07G-K08-5060-R	DFN5060-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT100N07G-K08-5060-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) K08-5060: DFN5060-8
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V _{DSS}	65	V
Gate-Source Voltage			V _{GSS}	+20 / -12	V
Drain Current	Continuous	T _C =25°C	I _D	100	A
		T _C =100°C		63	A
	Pulsed (Note 2)		I _{DM}	400	A
Avalanche Energy (Note 3)		Single Pulsed	E _{AS}	245	mJ
Power Dissipation			P _D	142	W
Junction Temperature			T _J	+150	°C
Storage Temperature			T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=70\text{A}$, $V_{DD}=25\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD}\leq 3.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62	$^\circ\text{C}/\text{W}$
Junction to Case		θ_{JC}	0.88	$^\circ\text{C}/\text{W}$

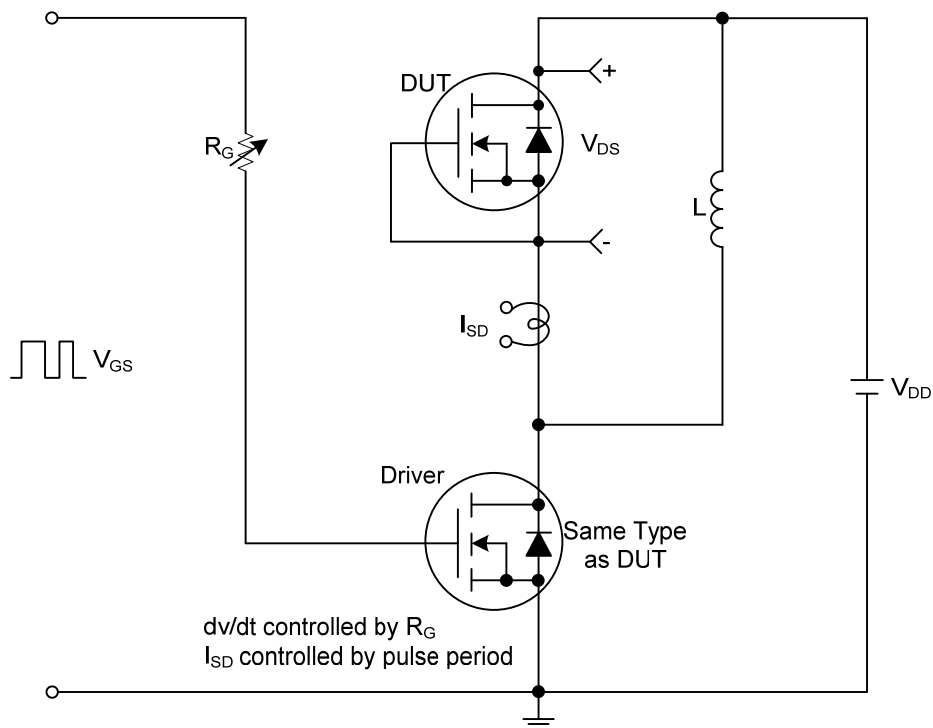
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	65			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
			V _{DS} =48V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A		2.3	2.8	mΩ
			V _{GS} =4.5V, I _D =10A		4.2	5.4	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		4780	9500	pF
Output Capacitance		C _{OSS}			1365	2700	pF
Reverse Transfer Capacitance		C _{RSS}			51	102	pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =48V, V _{GS} =10V, I _D =10A		59	120	nC
Gate to Source Charge		Q _{GS}			10.4	20	nC
Gate to Drain Charge		Q _{GD}			19.6	38	nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =30V, V _{GS} =10V, I _D =6.0A, R _G =1.0Ω		22	44	ns
Rise Time		t _R			14	28	ns
Turn-off Delay Time		t _{D(OFF)}			40	80	ns
Fall-Time		t _F			20	40	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				100	A
Maximum Body-Diode Pulsed Current		I _{SM}				200	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =1.0A, V _{GS} =0V			1.0	V

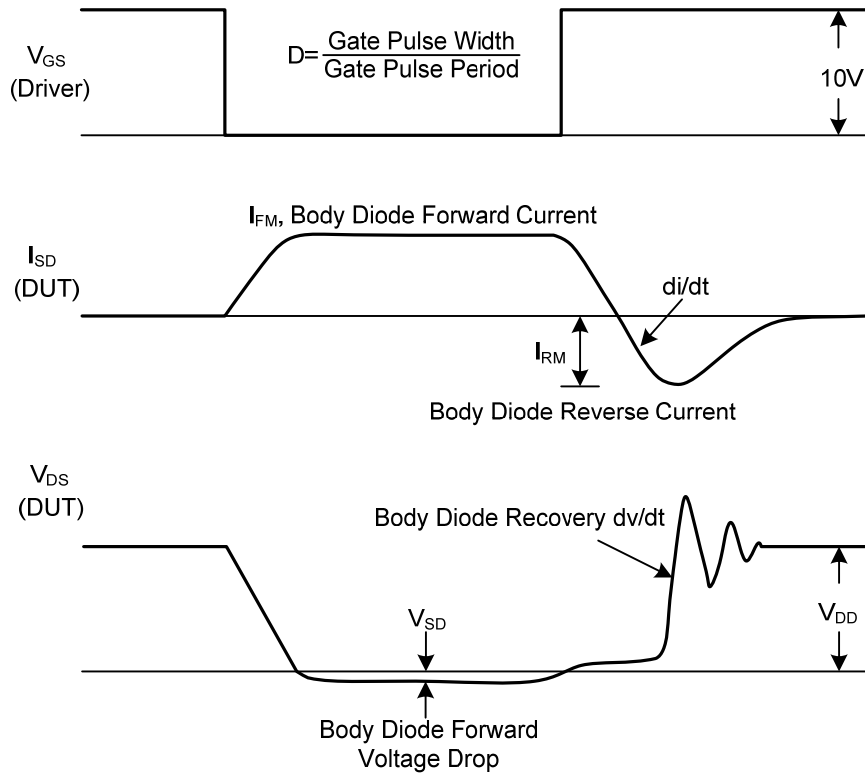
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



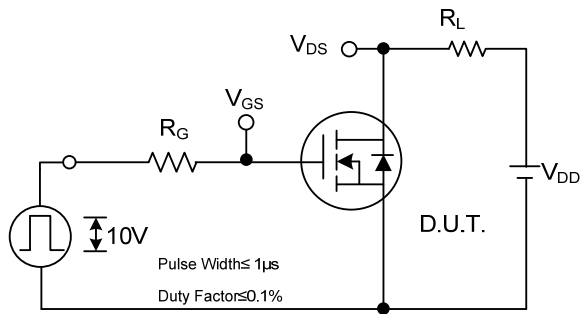
Peak Diode Recovery dv/dt Test Circuit



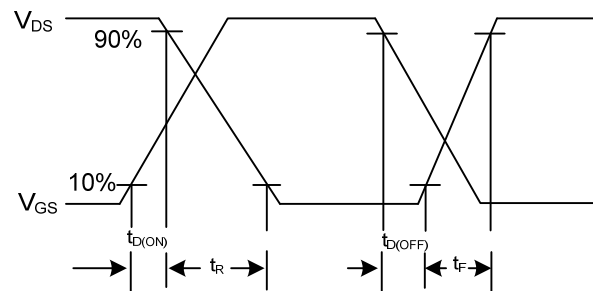
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

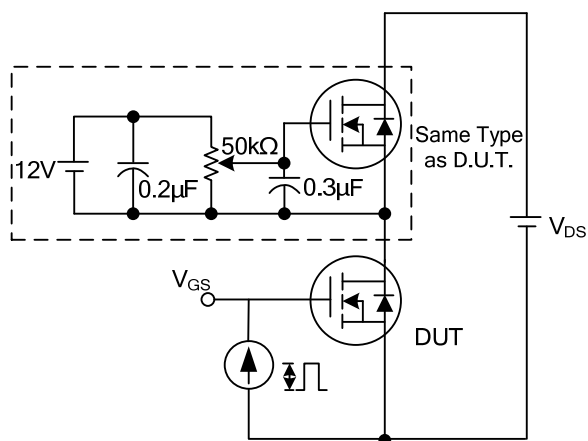
■ TEST CIRCUITS AND WAVEFORMS



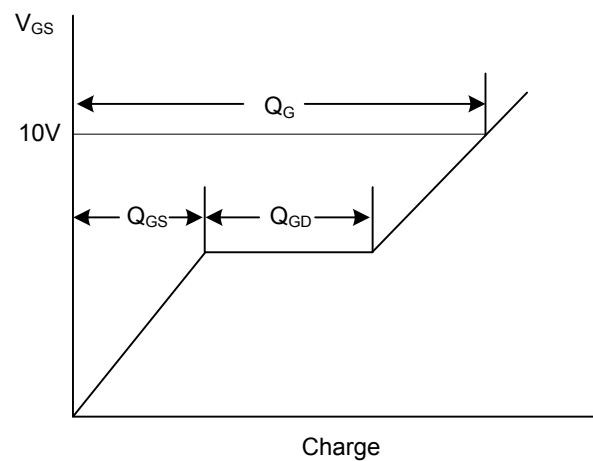
Switching Test Circuit



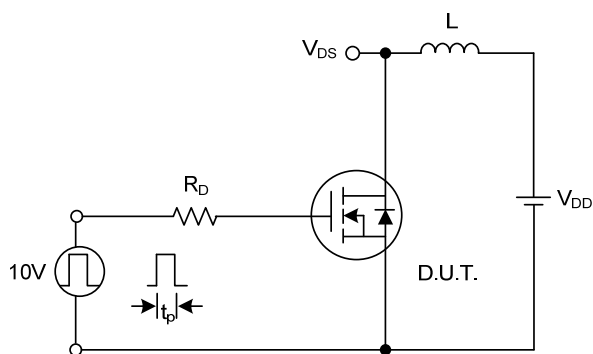
Switching Waveforms



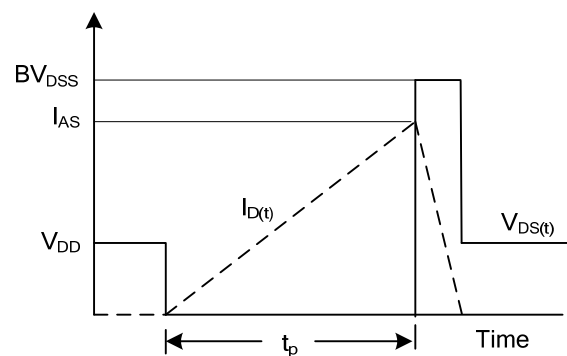
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

TYPICAL CHARACTERISTICS

Fig.1 Continuous Drain Current vs. Case Temperature

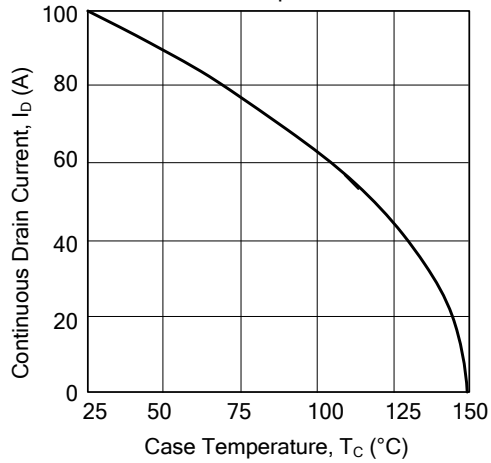


Fig.2 Normalized $R_{DS(on)}$ vs. Junction Temperature

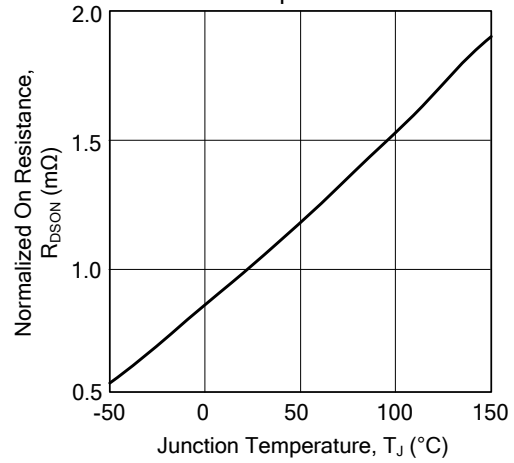


Fig.3 Normalized V_{th} vs. Junction Temperature

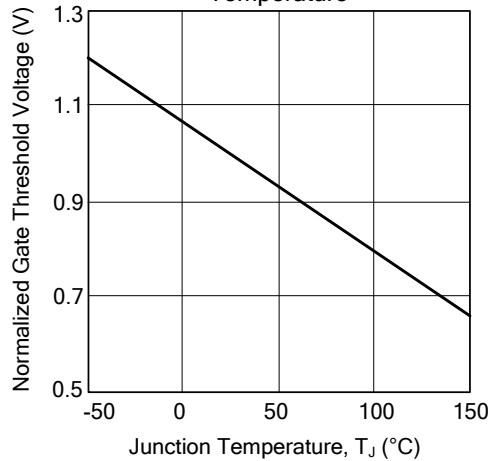


Fig.4 Gate Charge Waveform

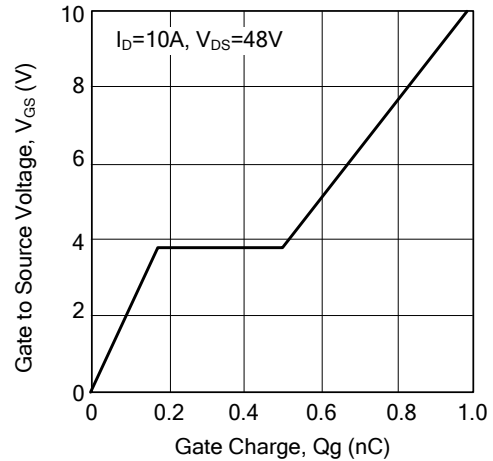


Fig.5 Normalized Transient Impedance

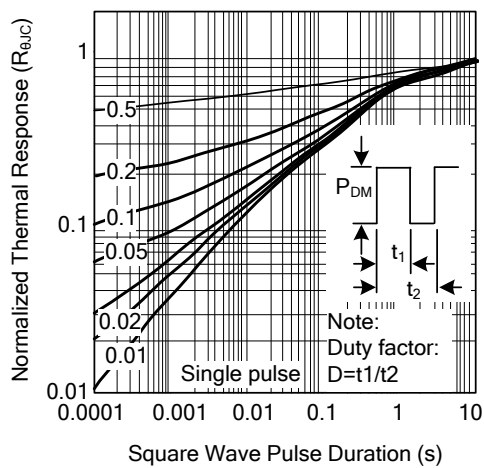
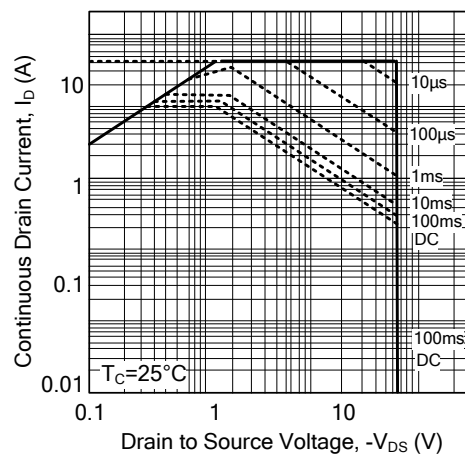


Fig.6 Maximum Safe Operation Area



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