

**60NM65**

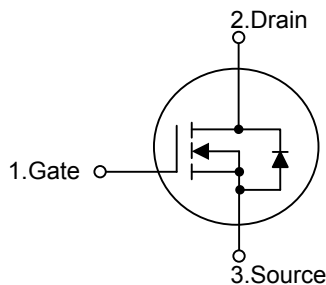
Preliminary

Power MOSFET**60A, 650V N-CHANNEL
SUPER-JUNCTION MOSFET****DESCRIPTION**

The **UTC 60NM65** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at DC-DC, AC-DC converters for power applications.

FEATURES

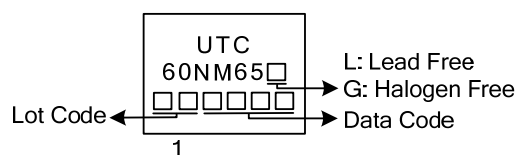
- * $R_{DS(ON)} < 0.065\Omega$ @ $V_{GS}=10V$, $I_D=30A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
60NM65L-T3P-T	60NM65G-T3P-T	TO-3P	G	D	S	Tube
60NM65L-T47-T	60NM65G-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

60NM65L-T3P-T (1)Packing Type (2)Package Type (3)Green Package		(1) T: Tube (2) T3P: TO-3P, T47: TO-247 (3) L: Lead Free, G: Halogen Free and Lead Free
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MARKING

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	60	A
	Pulsed (Note 2)	I_{DM}	240	A
Avalanche Current (Note 2)		I_{AR}	10	A
Avalanche Energy		E_{AS}	1800	mJ
Peak Diode Recovery dv/dt		dv/dt	9	V/ns
Power Dissipation	TO-247	P_D	310	W
	TO-3P		357	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 36\text{mH}$, $I_{AS} = 10\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-247	θ_{JA}	40	$^{\circ}\text{C}/\text{W}$
	TO-3P		30	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-247	θ_{JC}	0.4	$^{\circ}\text{C}/\text{W}$
	TO-3P		0.35	$^{\circ}\text{C}/\text{W}$

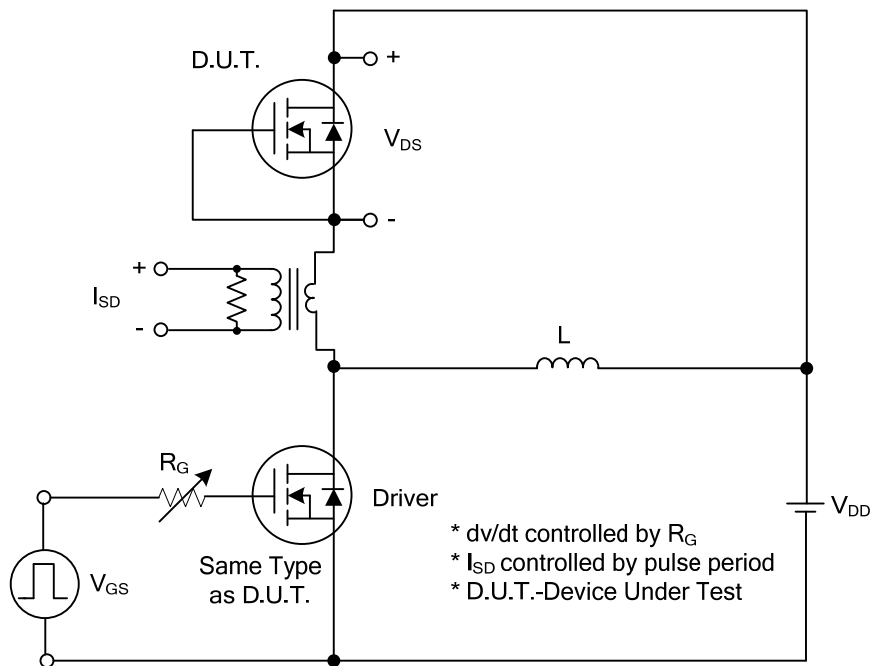
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	650			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =650V, V _{GS} =0V			50	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =30A			0.065	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		5400		pF
Output Capacitance		C _{OSS}			2500		pF
Reverse Transfer Capacitance		C _{RSS}			70		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =50V, V _{GS} =10V, I _D =1.3A I _G = 100μA (Note1, 2)		600		nC
Gate to Source Charge		Q _{GS}			20		nC
Gate to Drain Charge		Q _{GD}			95		nC
Turn-ON Delay Time (Note 1)		t _{D(ON)}	V _{DS} =30V, V _{GS} =10V, I _D =0.5A, R _G =25Ω (Note1, 2)		150		ns
Rise Time		t _R			475		ns
Turn-OFF Delay Time		t _{D(OFF)}			1450		ns
Fall-Time		t _F			850		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				60	A
Maximum Body-Diode Pulsed Current		I _{SM}				240	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =60A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)		t _{rr}	I _S =30A, V _{GS} =0V,		650		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dl _F /dt=100A/μs (Note 1)		14		μC

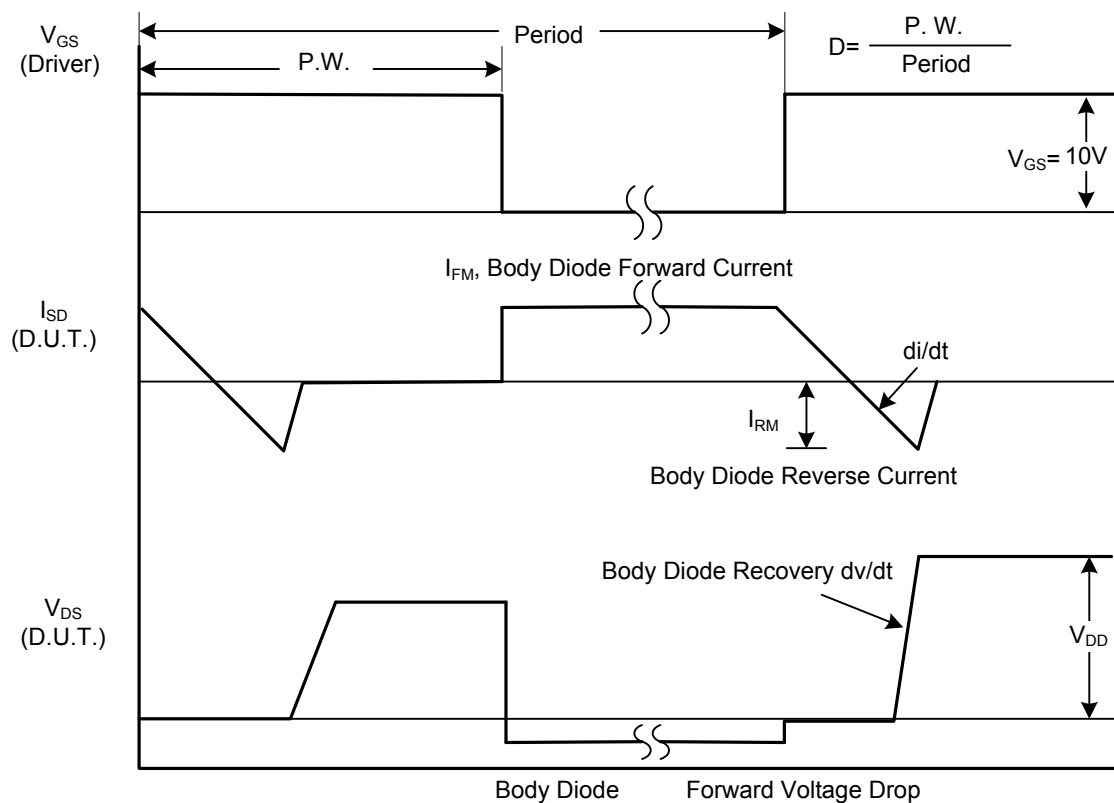
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



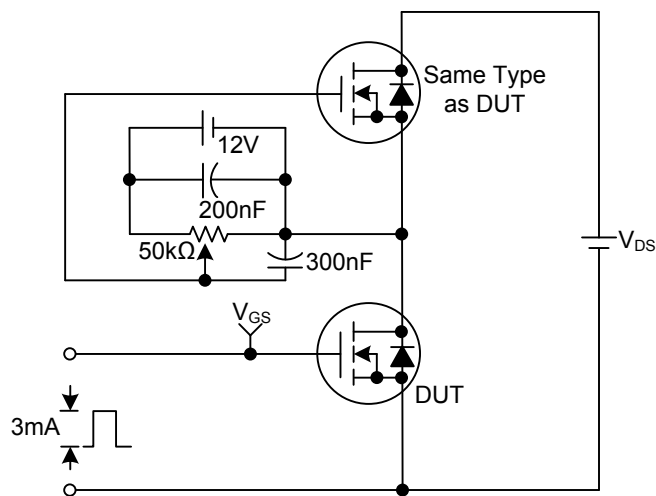
Peak Diode Recovery dv/dt Test Circuit



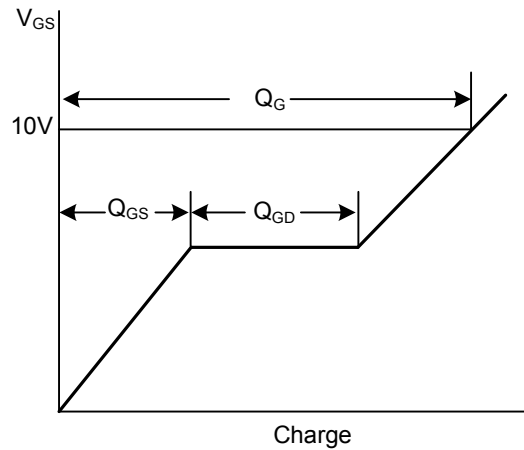
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

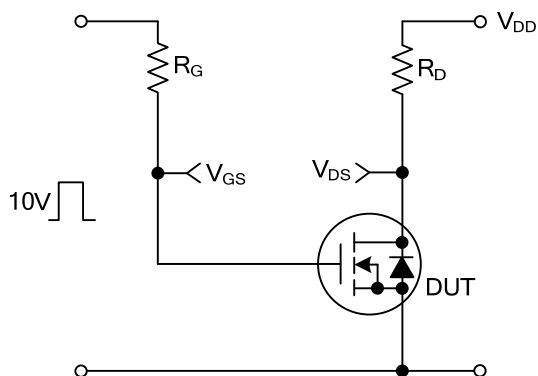
Gate Charge Test Circuit



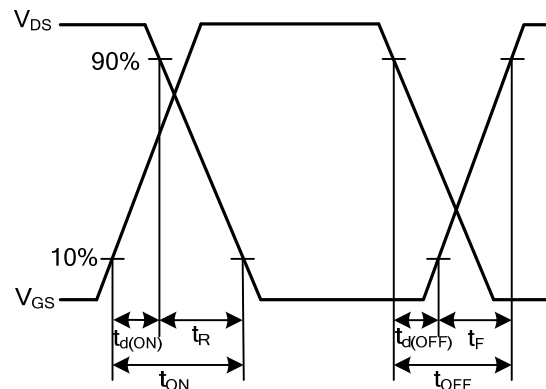
Gate Charge Waveforms



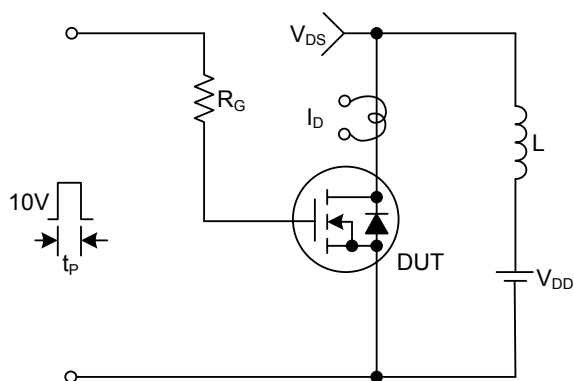
Resistive Switching Test Circuit



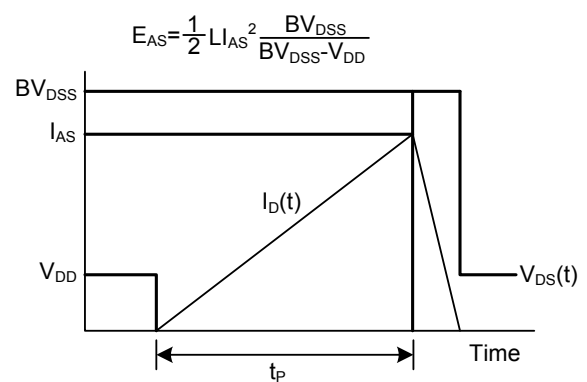
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



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