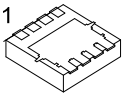
30V, 34A N-CHANNEL ENHANCEMENT MODE POWER MOSFET



DFN3030-8

■ DESCRIPTION

The UTC **UT7430** is an N-Channel MOSFET, it uses UTC's advanced technology to provide customers with a minimum on-state resistance, high switching speed and low gate charge.

The UTC **UT7430** is suitable for general purpose applications and high side switch in SMPS.

■ FEATURES

* $R_{DS(ON)}$<12mΩ @ V_{GS}=10V, I_D=20A
  $R_{DS(ON)}$<16mΩ @ V_{GS}=4.5V, I_D=20A
* Low gate charge
* High switching speed

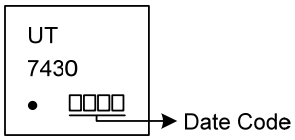
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT7430G-K08-3030-R	UT7430G-K08-3030-R	DFN3030-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT7430G-K08-3030-R (1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) K08-3030: DFN3030-8
(3)Green Package	(3) G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Drain Current	Continuous	T_C=25°C	I_D	34	A
		T_C=100°C		21	A
	Pulsed (Note 3)		I_{DM}	80	A
Continuous Drain Current (Note 1)		T_A=25°C	I_{DSM}	13	A
		T_A=70°C		10.2	A
Avalanche Current (Note 3)			I_{AR}	22	A
Repetitive Avalanche Energy		L=0.1mH (Note 3)	E_{AR}	24	mJ
Power Dissipation (Note 2)		T_C=25°C	P_D	23	W
		T_C=100°C		9	W
Power Dissipation (Note 1)		T_A=25°C	P_{DSM}	3.1	W
		T_A=70°C		2	W
Junction Temperature			T_J	-55~+150	°C
Storage Temperature Range			T_{STG}	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction to Ambient (Note 1)	θ_{JA}		60	75	°C/W
Junction to Case (Note 2)	θ_{JC}		4.5	5.4	°C/W

Notes: 1. The value of θ_{JA} is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

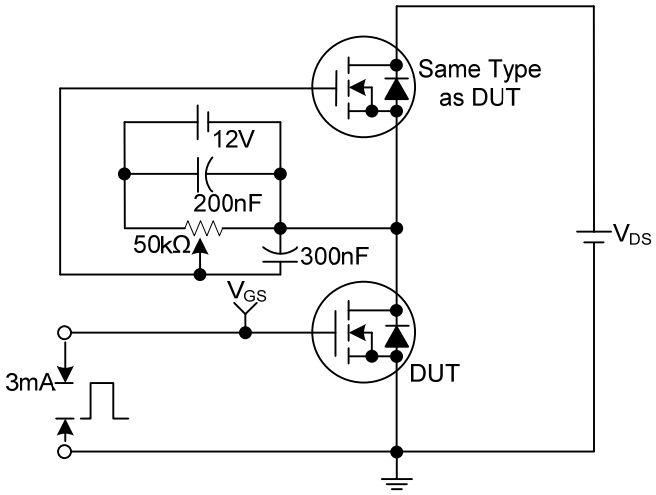
2. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

3. Repetitive rating, pulse width limited by junction temperature $T_{J\ (MAX)}$=150°C.

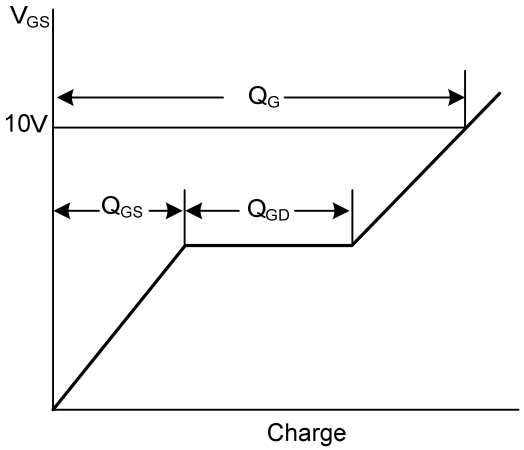
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.5	1.9	2.5	V
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		10	12	mΩ
			V_{GS}=4.5V, I_D=20A		13	16	mΩ
Forward Transconductance		g_{FS}	V_{DS}=5V, I_D=20A		45		S
On State Drain Current		$I_{D(ON)}$	V_{GS}=10V, V_{DS}=5V	80			A
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=15V, f=1.0MHz		780		pF
Output Capacitance		C_{OSS}			200		pF
Reverse Transfer Capacitance		C_{RSS}			165		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{GS}=4.5V, V_{DS}=15V, I_D=20A		15.2		nC
Total Gate Charge		Q_G	V_{GS}=10V, V_{DS}=15V, I_D=20A		32.7		nC
Gate to Source Charge		Q_{GS}			7.6		nC
Gate to Drain Charge		Q_{GD}			7.2		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		16		ns
Rise Time		t_R			33		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			45		ns
Fall-Time		t_F			18		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				25	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=1A, V_{GS}=0V		0.7	1	V

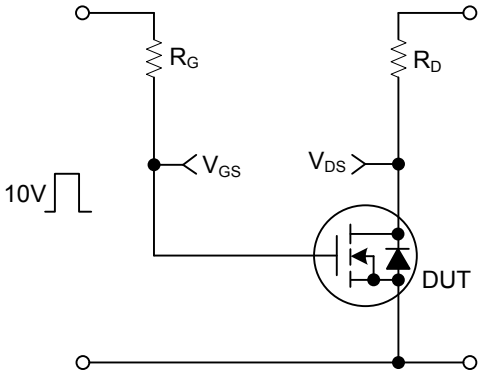
■ TEST CIRCUITS AND WAVEFORMS



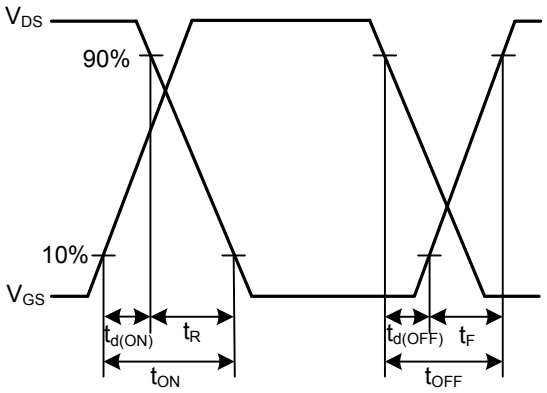
Gate Charge Test Circuit



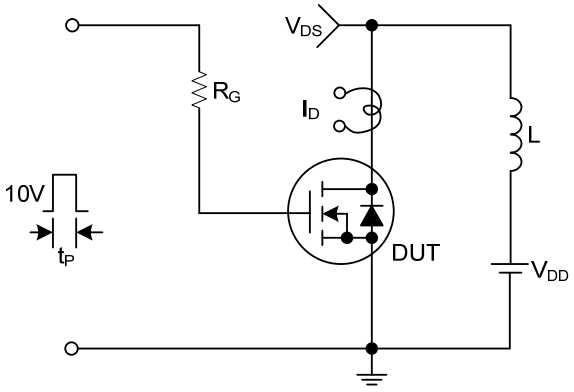
Gate Charge Waveforms



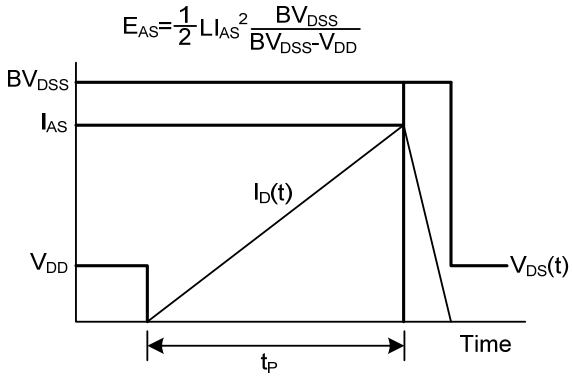
Resistive Switching Test Circuit



Resistive Switching Waveforms

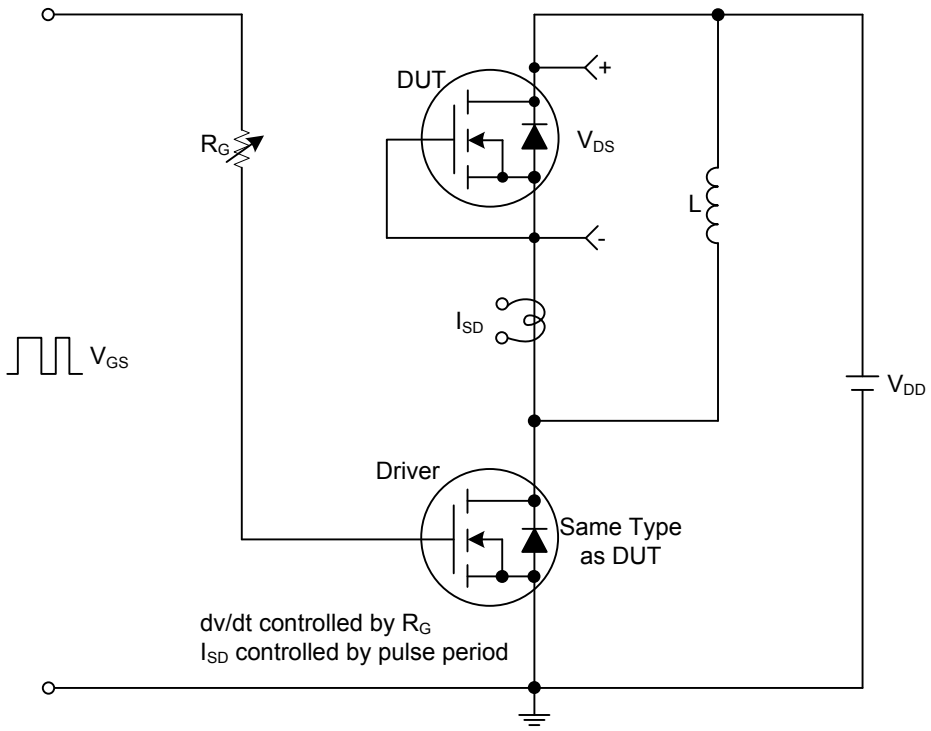


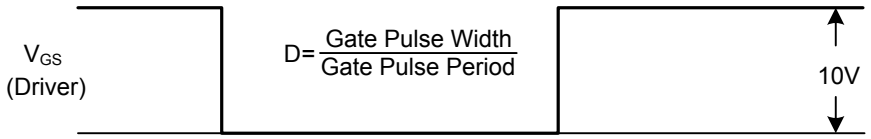
Unclamped Inductive Switching Test Circuit

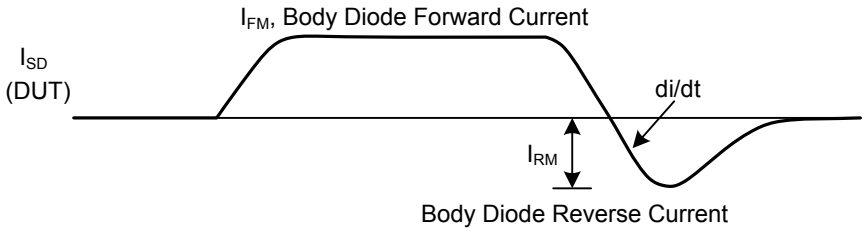


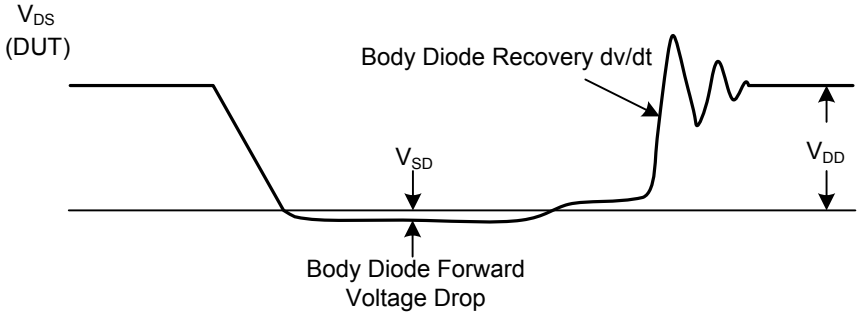
Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS









Peak Diode Recovery dv/dt Test Circuit and Waveforms