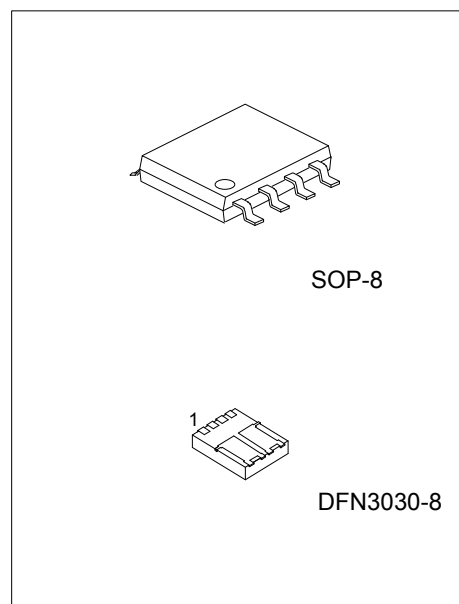
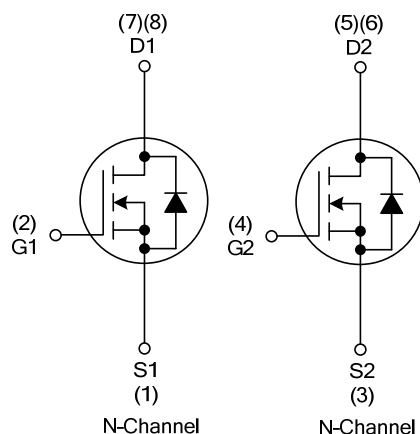


**UTT12NN10****Power MOSFET****2.5A, 100V DUAL N-CHANNEL
ENHANCEMENT MODE
POWER MOSFET****DESCRIPTION**

The UTC **UTT12NN10** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(on)}$ characteristic by high cell density trench technology.

FEATURES

- * $R_{DS(ON)} < 0.28\Omega$ @ $V_{GS}=10V$, $I_D=2.0A$
- * Fast Switching Speed
- * Simple Drive Requirement

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT12NN10L-S08-R	UTT12NN10G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel
UTT12NN10L-K08-3030-R	UTT12NN10G-K08-3030-R	DFN3030-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT12NN10G-S08-R		(1) Packing Type	(1) R: Tape Reel (2) S08: SOP-8, K08-3030: DFN3030-8 (3) G: Halogen Free and Lead Free, L: Lead Free
		(2) Package Type	
		(3) Green Package	

■ MARKING

SOP-8	DFN3030-8
Diagram of SOP-8 marking: The package has pins numbered 1 to 8. The marking includes 'UTC' and 'UTT12NN10'. A date code (four digits) is located at the top right, and a lot code (two digits) is at the bottom right, both indicated by arrows.	Diagram of DFN3030-8 marking: The package has the marking 'UTT' and '12NN10'. A date code (four digits) is located at the bottom right, indicated by an arrow.

■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	2.5	A
	Pulsed (Note 2)	I_{DM}	10	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	2.3	V/nS
Power Dissipation	SOP-8	P_D	1.6	W
	DFN3030-8		2.0	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $I_{SD} \leq 2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DS}$, $T_J = 25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	78	$^{\circ}\text{C}/\text{W}$
	DFN3030-8		62.5	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

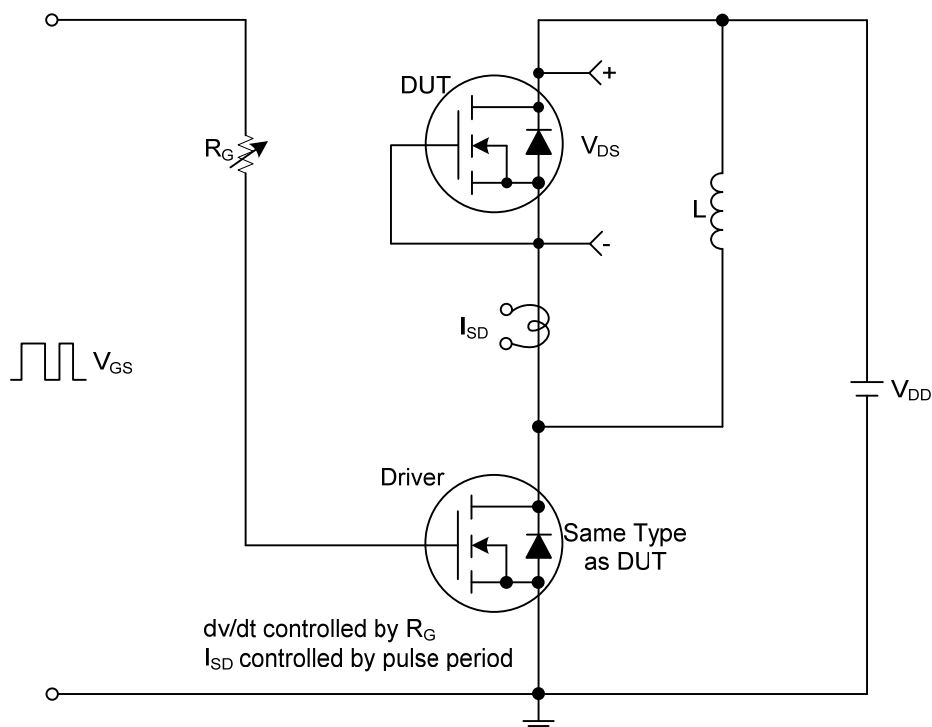
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	100			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{DS} =0V, V _{GS} =20V			100	nA
	Reverse		V _{DS} =0V, V _{GS} =-20V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2A			0.28	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		400		pF
Output Capacitance		C _{OSS}			33		pF
Reverse Transfer Capacitance		C _{RSS}			26		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =50V, V _{GS} =10V, I _D =1.3A, I _D =100μA (Note 1, 2)		40		nC
Gate-Source Charge		Q _{GS}			2.0		nC
Gate-Drain Charge		Q _{GD}			3.0		nC
Turn-ON Delay Time (Note 1)		t _{D(ON)}	V _{DS} =30V, V _{GS} =10V, I _D =0.5A, R _G =25Ω (Note 1, 2)		29		ns
Turn-ON Rise Time		t _R			26		ns
Turn-OFF Delay Time		t _{D(OFF)}			165		ns
Turn-OFF Fall Time		t _F			37		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				2.5	A
Maximum Body-Diode Pulsed Current		I _{SM}				10	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =1.5A, V _{GS} =0V			1.3	V
Body Diode Reverse Recovery Time (Note 1)		t _{rr}	I _S =2.0A, V _{GS} =0V,		210		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=50A/μs		170		nC

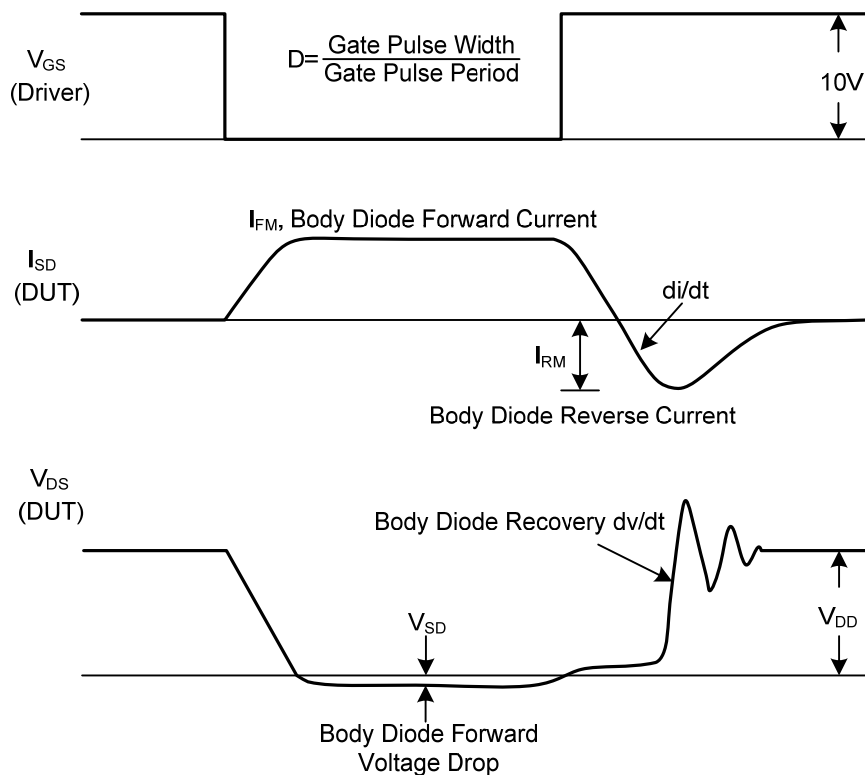
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



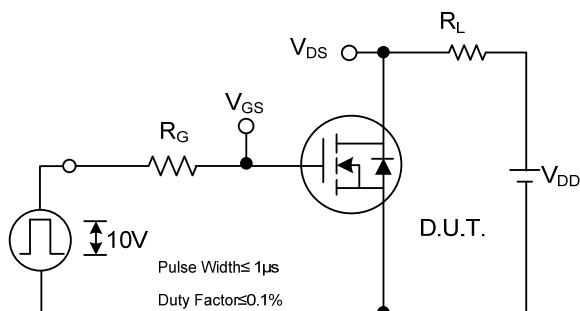
Peak Diode Recovery dv/dt Test Circuit



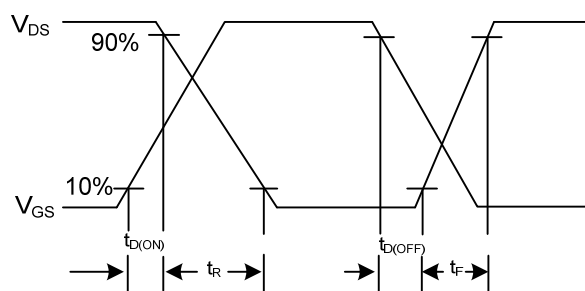
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

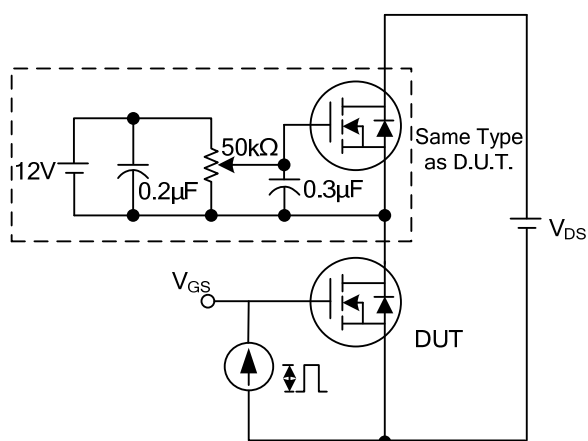
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



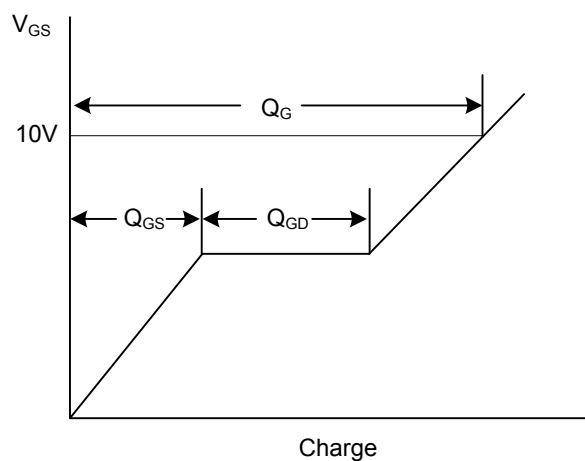
Switching Test Circuit



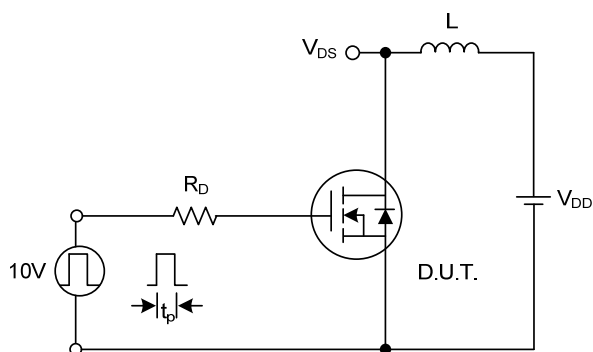
Switching Waveforms



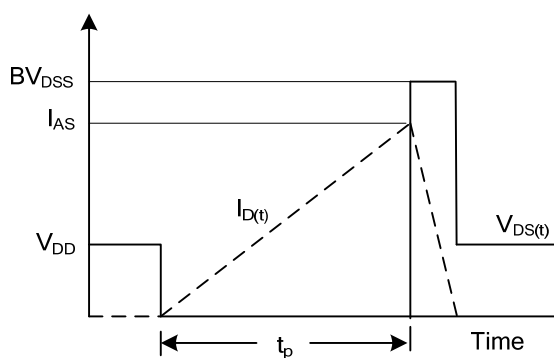
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.