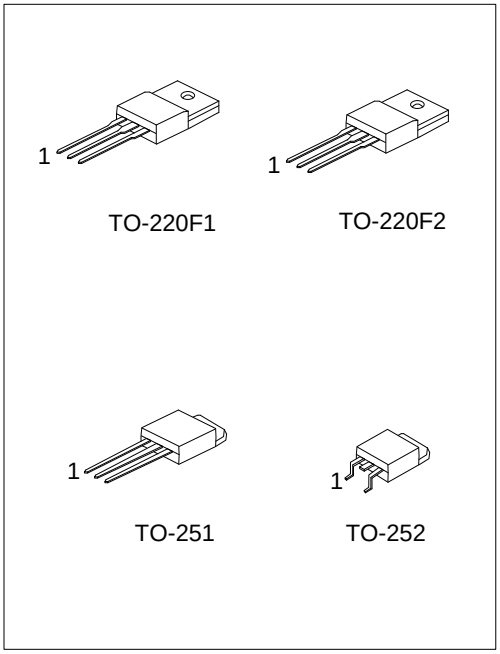
6N40-TC

Power MOSFET

6A, 400V N-CHANNEL POWER MOSFET



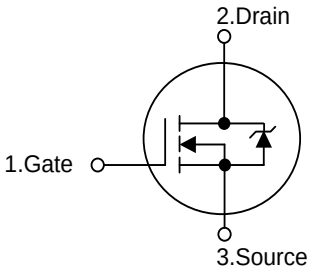
■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ FEATURES

* $R_{DS(ON)} \leq 1.1\ \Omega$ @ V_{GS}=10V, I_D=3.0A
* Avalanche Energy Specified
* Fast Switching Capability
* Linear Transfer Characteristics
* High Input Impedance

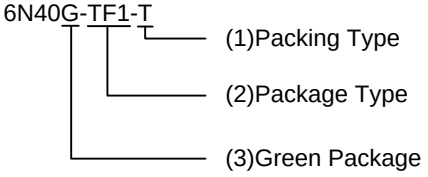
■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
6N40L-TF1-T	6N40G-TF1-T	TO-220F1	G	D	S	Tube
6N40L-TF2-T	6N40G-TF2-T	TO-220F2	G	D	S	Tube
6N40L-TM3-T	6N40G-TM3-T	TO-251	G	D	S	Tube
6N40L-TN3-R	6N40G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

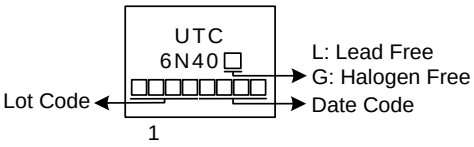


(1) T: Tube, R: Tape Reel

(2) TF1: TO-220F1, TF2: TO-220F2, TM3: TO-251
TN3: TO-252

(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	400	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	6	A
	Pulsed (Note 2)	I_{DM}	12	A
Avalanche Current (Note 2)		I_{AR}	4.6	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	106	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.0	V/ns
Power Dissipation	TO-220F1/TO-220F2	P_D	28	W
	TO-251/TO-252		48	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L = 10mH, I_{AS} = 4.6A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤5.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220F1/TO-220F2	θ_{JA}	62.5	°C/W
	TO-251/TO-252		110	°C/W
Junction to Case	TO-220F1/TO-220F2	θ_{JC}	4.4	°C/W
	TO-251/TO-252		2.6 (Note)	°C/W

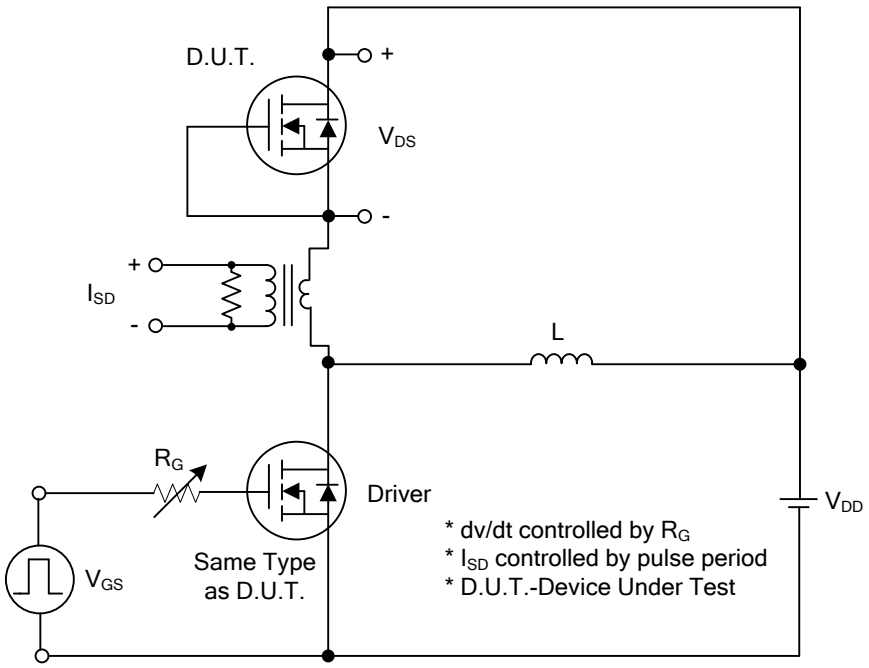
Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

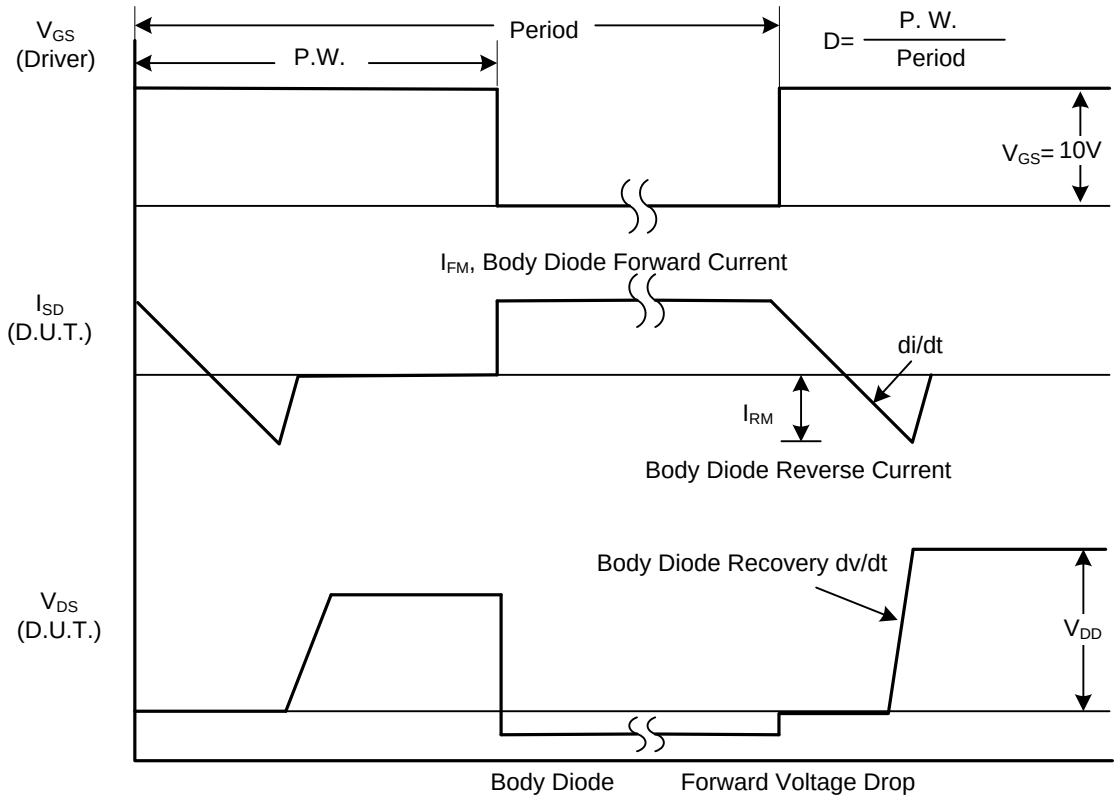
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	400			V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=Rated BV_{DSS}, V_{GS}=0V			25	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=3.0A			1.1	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{GS}=0V,V_{DS}=25V, f=1.0MHz		500		pF
Output Capacitance	C_{OSS}			70		pF
Reverse Transfer Capacitance	C_{RSS}			7		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	V_{DS}=320V, V_{GS}=10V, I_D=6A I_G=1mA (Note1, 2)		12		nC
Gate to Source Charge	Q_{GS}			3.5		nC
Gate to Drain Charge	Q_{GD}			3		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	V_{DS}=100V, V_{GS}=10V, I_D=6A, R_G=25Ω (Note1, 2)		6		ns
Rise Time	t_R			18		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			32		ns
Fall-Time	t_F			25		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				6	A
Maximum Body-Diode Pulsed Current	I_{SM}				12	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	I_S=6.0A, V_{GS}=0V			1.6	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	I_S=6.0A, V_{GS}=0V dI_F/dt=100A/μs		180		ns
Body Diode Reverse Recovery Charge	Q_{rr}			2.3		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

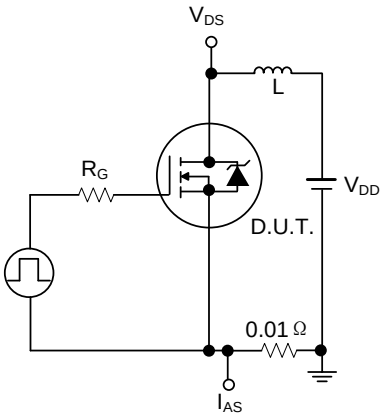


Figure 1A. Unclamped Energy Test Circuit

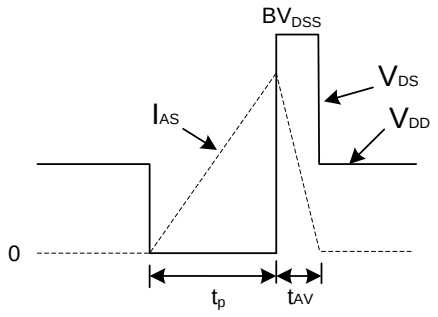


Figure 1B. Unclamped Energy Waveforms

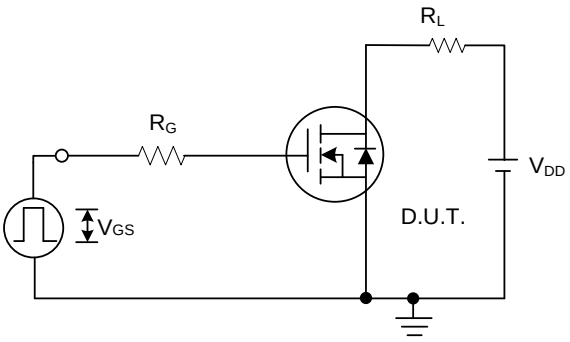


Figure 2A. Switching Time Test Circuit

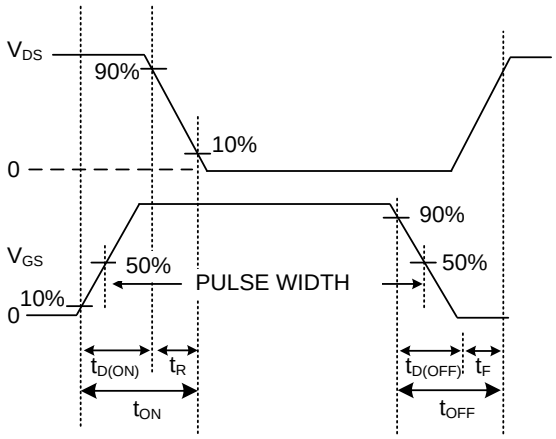


Figure 2B. Resistive Switching Waveforms

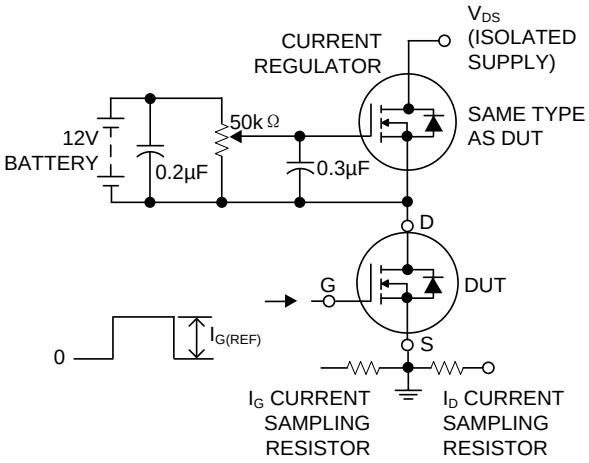


Figure 3A. Gate Charge Test Circuit

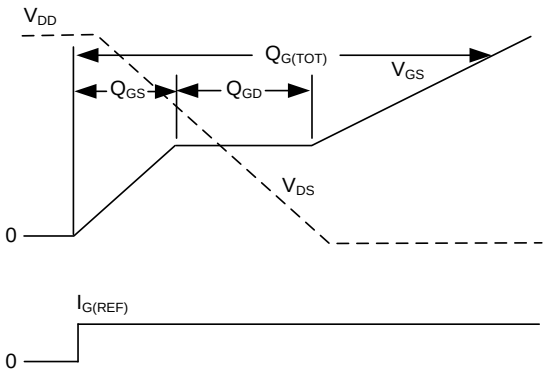


Figure 3B. Gate Charge Waveforms