

**UD4509-H***Power MOSFET***DUAL ENHANCEMENT MODE
(N-CHANNEL/P-CHANNEL)****DESCRIPTION**

The UTC **UD4509-H** is an N & P-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with a minimum on-state resistance, high switching speed and low gate charge.

The UTC **UD4509-H** is suitable for low voltage applications such as DC/DC converters.

FEATURES

* N-channel: 30V/28A

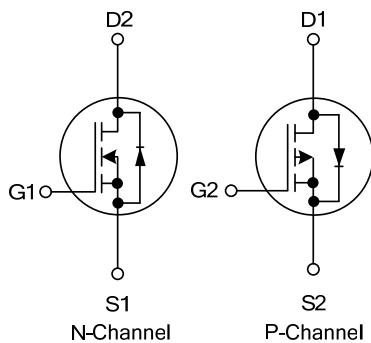
$R_{DS(on)} < 10m\Omega @ V_{GS}=10V$

* P-channel: -30V/-25A

$R_{DS(on)} < 21m\Omega @ V_{GS}=-10V$

* High switching speed

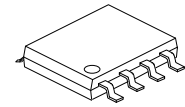
* Low gate charge

SYMBOL**ORDERING INFORMATION**

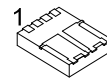
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1.	2.	3.	4.	5.	6.	7.	8.	
UD4509L-S08-R	UD4509G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel
UD4509L-K08-5060-R	UD4509G-K08-5060-R	DFN5060-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UD4509G-S08-R		(1)Packing Type	(1) R: Tape Reel
		(2)Package Type	(2) S08: SOP-8, K08-5060: DFN5060-8
		(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

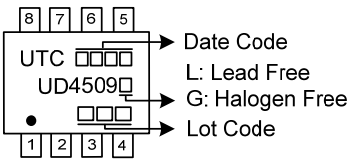
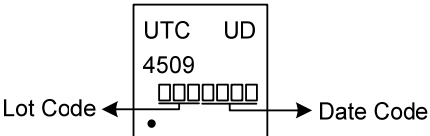


SOP-8



DFN5060-8

MARKING

SOP-8	DFN5060-8
 The diagram shows the marking layout for an SOP-8 package. It is a rectangular package with pins 1 through 8. The marking area contains the text 'UTC' followed by three empty boxes, 'UD4509' followed by one empty box, and a dot followed by two empty boxes. Arrows point from these areas to labels: 'Date Code' for the first three boxes, 'L: Lead Free' and 'G: Halogen Free' for the 'UD4509' area, and 'Lot Code' for the last two boxes.	 The diagram shows the marking layout for a DFN5060-8 package. It is a small rectangular package. The marking area contains the text 'UTC' followed by 'UD', '4509' followed by one empty box, and a dot followed by five empty boxes. Arrows point from these areas to labels: 'Lot Code' for the first three boxes and 'Date Code' for the last five boxes.

■ ABSOLUTE MAXIMUM RATINGS ($T_J=25^\circ\text{C}$ unless otherwise specified)

PARAMETER			SYMBOL	RATINGS		UNIT
				N-channel	P-channe	
Drain-Source Voltage			V _{DSS}	30	-30	V
Gate-Source Voltage			V _{GSS}	±20	±20	V
Drain Current	Continuous (Note 3)	T _A =25°C	I _D	28	-25	A
		T _A =70		17.6	-15.7	A
	Pulsed (Note 1)		I _{DM}	56	-50	A
Power Dissipation	T _A =25°C	SOP-8	P _D	2		W
		DFN5060-8		3.8		W
Junction Temperature			T _J	-55 ~ +150		°C
Storage Temperature			T _{STG}	-55 ~ +150		°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 3)	SOP-8	θ_{JA}	62.5	$^\circ\text{C/W}$
	DFN5060-8		32.5	$^\circ\text{C/W}$

Note: Surface mounted on 1 in² copper pad of FR4 board ; 135 $^\circ\text{C/W}$ when mounted on Min. copper pad

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

N-channel

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250uA, V _{GS} =0V	30			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =24V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250uA	1		3	V
Static Drain-Source On-State Resistance (Note 2)		R _{DS(ON)}	V _{GS} =10V, I _D =10A			10	mΩ
			V _{GS} =4.5V, I _D =7A			16	mΩ
Forward Transconductance		g _{FS}	V _{GS} =10V, I _D =10A		20		S
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		715	1140	pF
Output Capacitance		C _{OSS}			220		pF
Reverse Transfer Capacitance		C _{RSS}			160		pF
Gate Resistance		R _G	f=1.0MHz		2.2		Ω
SWITCHING PARAMETERS							
Total Gate Charge (Note 2)		Q _G	V _{GS} =4.5V, V _{DS} =15V, I _D =10A		12	19.2	nC
Gate to Source Charge		Q _{GS}			2.5		nC
Gate to Drain Charge		Q _{GD}			7.5		nC
Turn-ON Delay Time (Note 2)		t _{D(ON)}	V _{DS} =15V, V _{GS} =10V, I _D =1A, R _G =3.3Ω, R _D =15Ω		9		ns
Rise Time		t _R			6.5		ns
Turn-OFF Delay Time		t _{D(OFF)}			23		ns
Fall-Time		t _F			9.5		ns
SOURCE TO DRAIN DIODE SPECIFICATIONS							
Drain-Source Diode Forward Voltage (Note 2)		V _{SD}	I _S =1.7A, V _{GS} =0V			1.2	V
Body Diode Reverse Recovery Time (Note 2)		t _{rr}	I _S =10A, V _{GS} =0V,		27		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dI/dt=100A/μs		18		nC

■ ELECTRICAL CHARACTERISTICS (CONT.)

P-channel

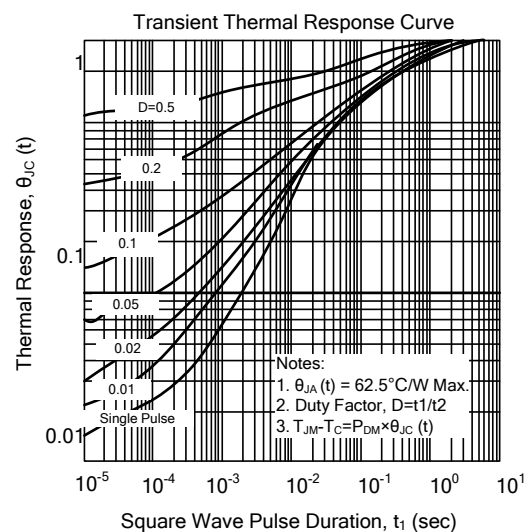
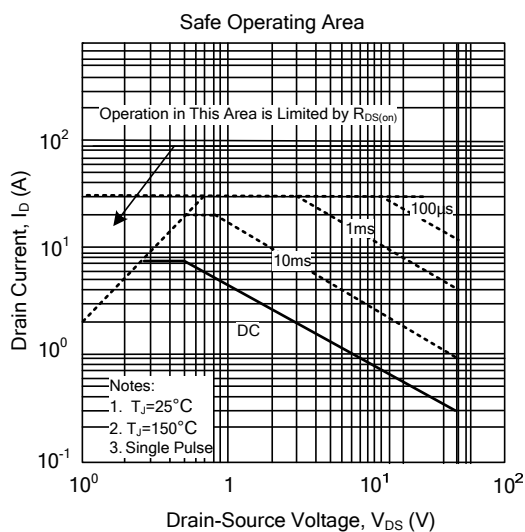
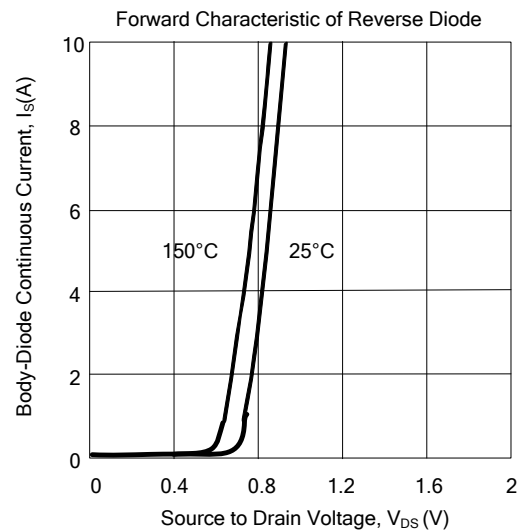
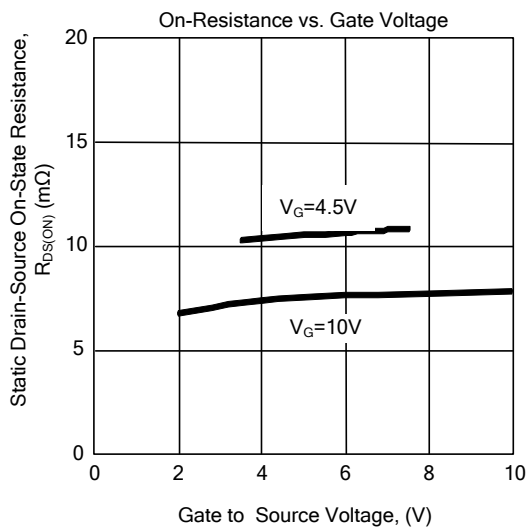
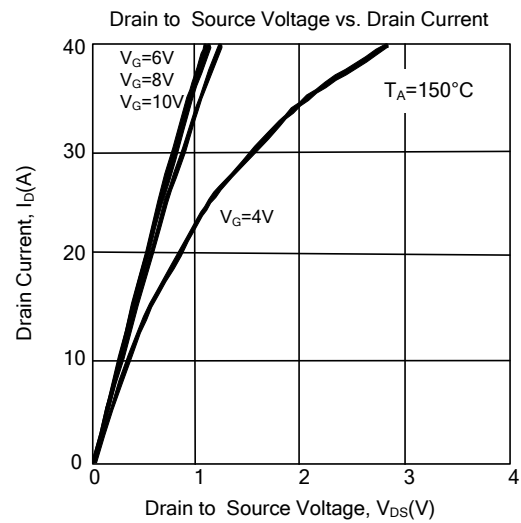
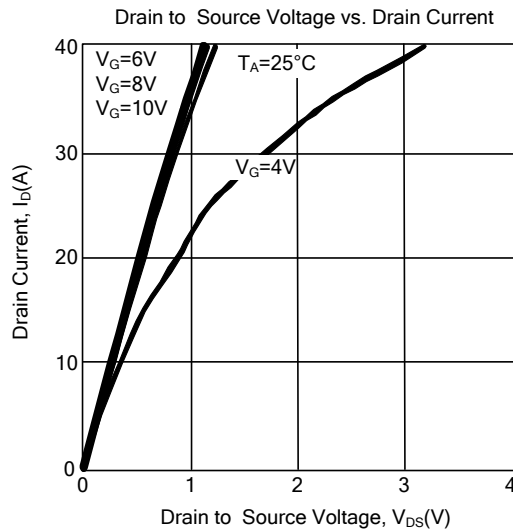
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =-250uA, V _{GS} =0V	-30			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-24V, V _{GS} =0V			-10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250uA	-1		-3	V
Static Drain-Source On-State Resistance (Note 2)		R _{DS(ON)}	V _{GS} =-10V, I _D =-7A			21	mΩ
			V _{GS} =-4.5V, I _D =-5A			32	mΩ
Forward Transconductance		g _{FS}	V _{GS} =-10V, I _D =-7A		15		S
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz		1260	2000	pF
Output Capacitance		C _{OSS}			210		pF
Reverse Transfer Capacitance		C _{RSS}			185		pF
Gate Resistance		R _G	f=1.0MHz		5.6		Ω
SWITCHING PARAMETERS							
Total Gate Charge (Note 2)		Q _G	V _{GS} =-4.5V, V _{DS} =15V, I _D =-7A		15	24	nC
Gate to Source Charge		Q _{GS}			3		nC
Gate to Drain Charge		Q _{GD}			8		nC
Turn-ON Delay Time (Note 2)		t _{D(ON)}	V _{DS} =15V, V _{GS} =-10V, I _D =-1A, R _G =3.3Ω, R _D =15Ω		10.5		ns
Rise Time		t _R			6.5		ns
Turn-OFF Delay Time		t _{D(OFF)}			40		ns
Fall-Time		t _F			29		ns
SOURCE TO DRAIN DIODE SPECIFICATIONS							
Drain-Source Diode Forward Voltage (Note 2)		V _{SD}	I _S =-1.7A, V _{GS} =0V			-1.2	V
Body Diode Reverse Recovery Time (Note 2)		t _{rr}	I _S =-7A, V _{GS} =0V,		22		ns
Body Diode Reverse Recovery Charge		Q _{rr}	di/dt=100A/μs		12		nC

Notes: 1. Pulse width limited by Max. junction temperature

2. Pulse test

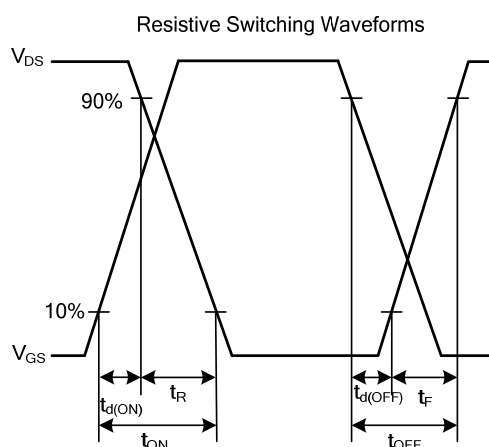
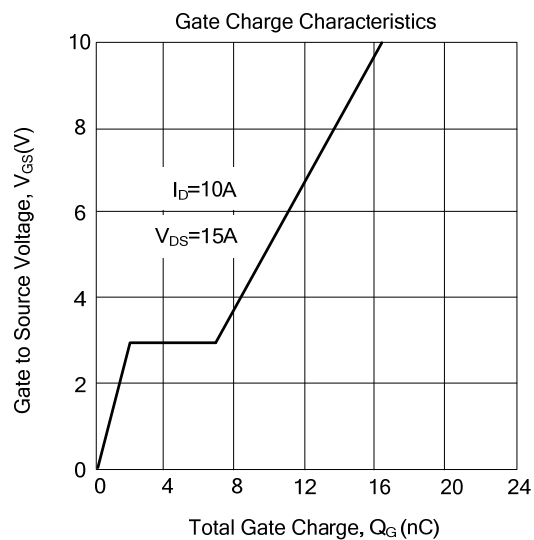
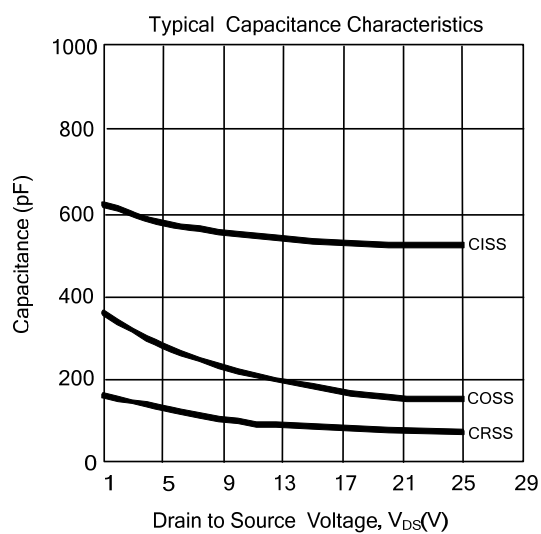
■ TYPICAL CHARACTERISTICS

N-CHANNEL



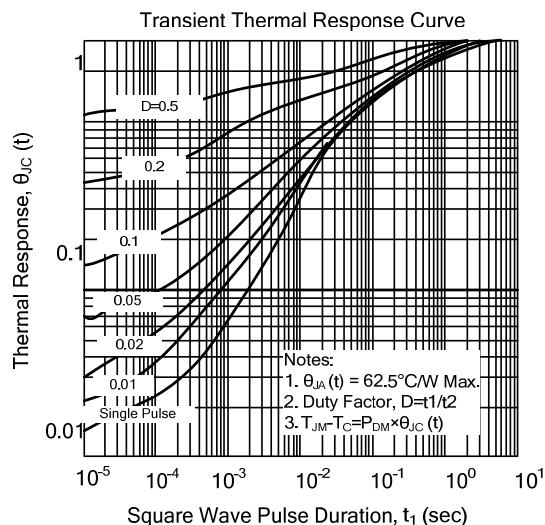
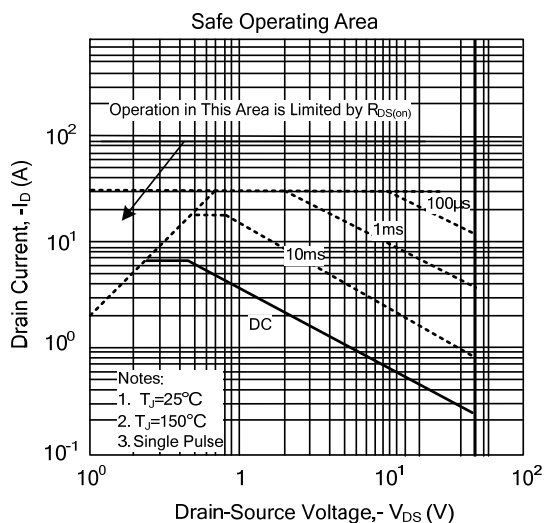
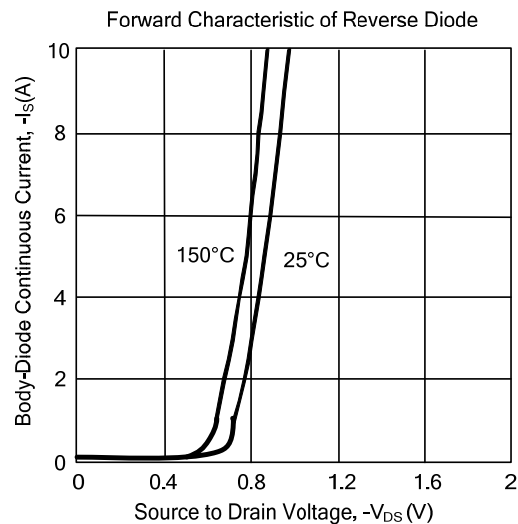
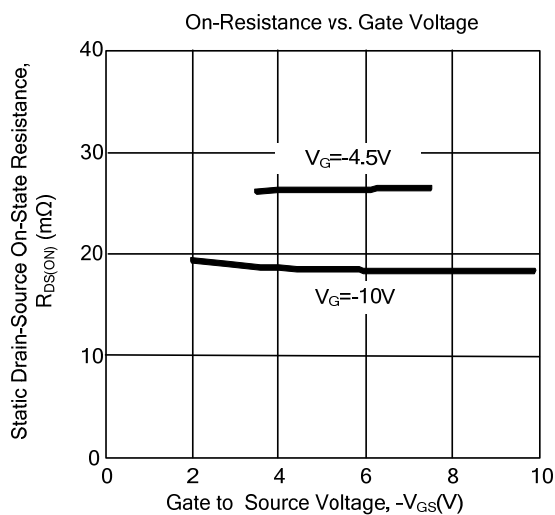
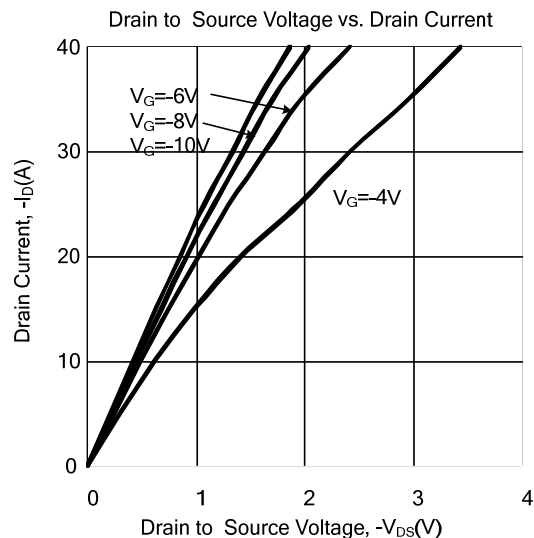
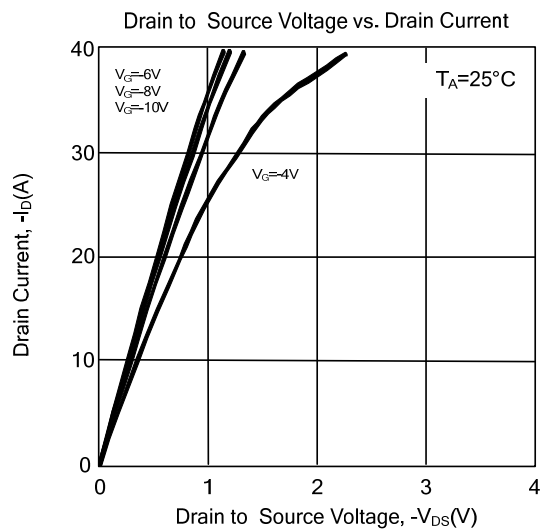
■ TYPICAL CHARACTERISTICS (Cont.)

N-CHANNEL



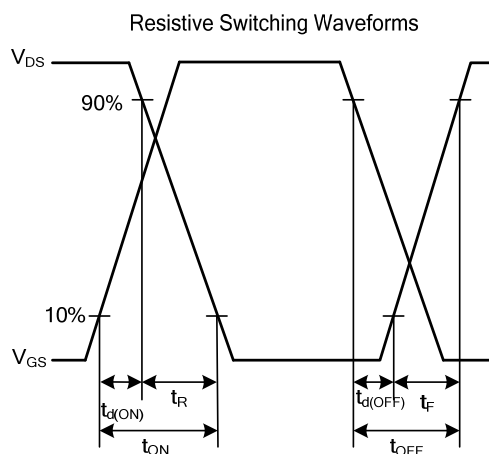
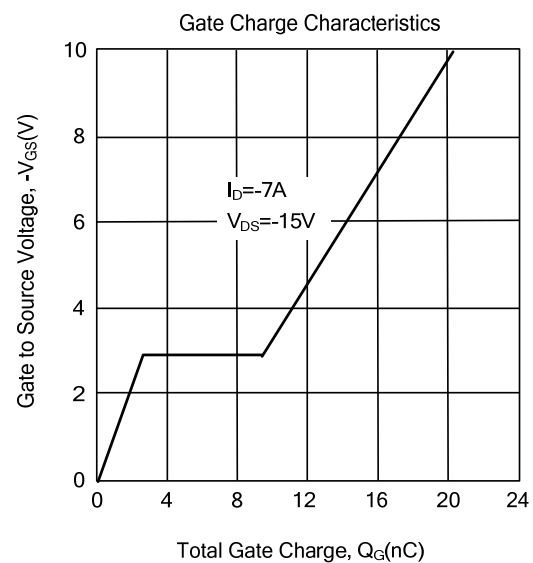
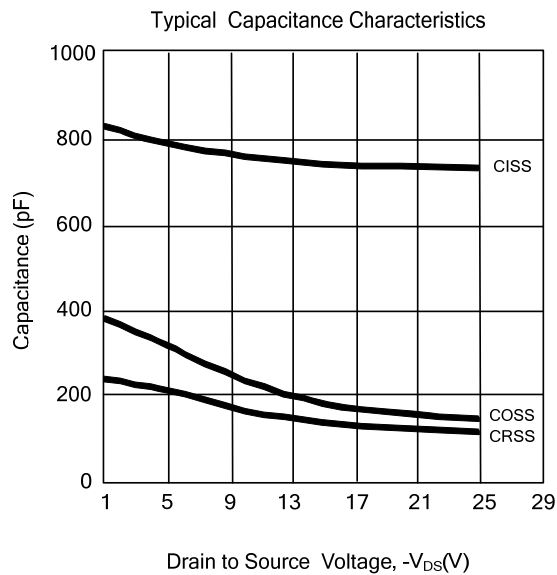
■ TYPICAL CHARACTERISTICS (Cont.)

P-CHANNEL



■ TYPICAL CHARACTERISTICS (Cont.)

P-CHANNEL



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