



5A, 650V N-CHANNEL SUPER-JUNCTION MOSFET

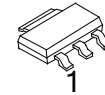
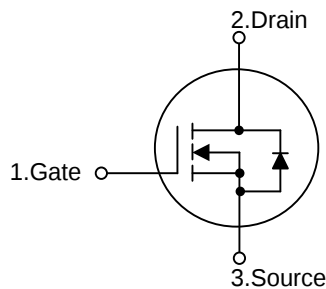
DESCRIPTION

The UTC 5NM65-U2 is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

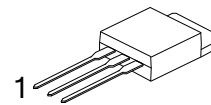
FEATURES

- * $R_{DS(on)} \leq 1.5 \Omega$ @ $V_{GS}=10V$, $I_D=2.5A$
- * Improved dv/dt capability
- * Fast switching
- * 100% avalanche tested

SYMBOL



SOT-223



TO-251

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5NM65G-AA3-R	5NM65G-AA3-R	SOT-223	G	D	S	Tape Reel
5NM65L-TM3-T	5NM65G-TM3-T	TO-251	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

5NM65G-TA3-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel, T: Tube (2) AA3: SOT-223, TM3: TO-251 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

SOT-223	TO-251
5NM65 Lot Code 1 L: Lead Free G: Halogen Free Date Code	UTC 5NM65 Lot Code 1 L: Lead Free G: Halogen Free Date Code

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	5.0	A
	Pulsed (Note 2)	I_{DM}	20	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	140	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.8	V/ns
Power Dissipation	SOT-223	P_D	10	W
	TO-251		50	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 144\text{mH}$, $I_{AS} = 1.4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-223	θ_{JA}	150	$^\circ\text{C/W}$
	TO-251		110	$^\circ\text{C/W}$
Junction to Case	SOT-223	θ_{JC}	12.5 (Note)	$^\circ\text{C/W}$
	TO-251		2.5 (Note)	$^\circ\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

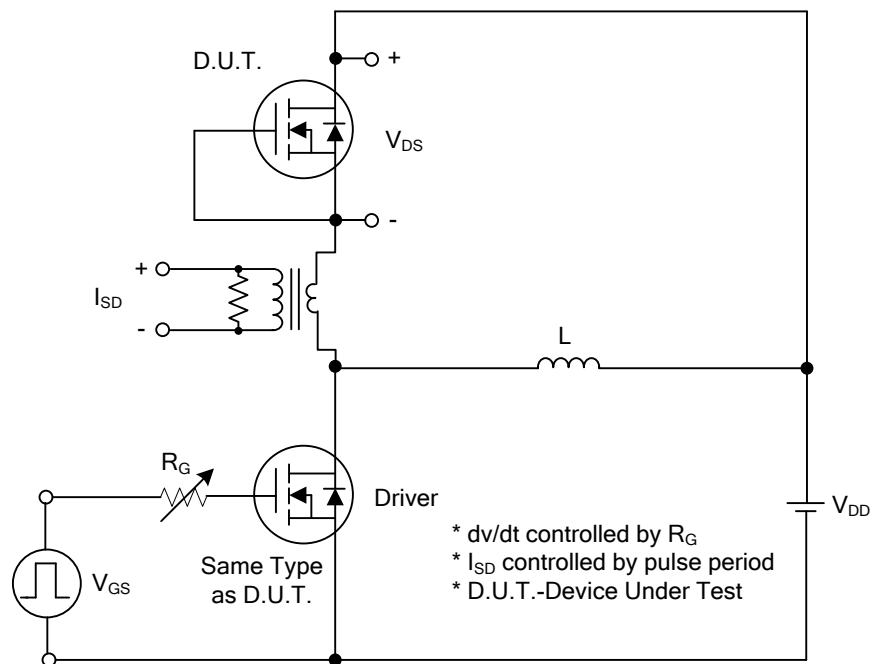
■ **ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	650			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =650V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2.5A			1.5	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		260		pF
Output Capacitance		C _{OSS}			140		pF
Reverse Transfer Capacitance		C _{RSS}			20		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =50V, V _{GS} =10V, I _D =1.3A, I _D =100μA (Note 1, 2)		77		nC
Gate to Source Charge		Q _{GS}			14		nC
Gate to Drain Charge		Q _{GD}			21		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =30V, V _{GS} =10V, I _D =0.5A, R _G =25Ω (Note 1, 2)		30		ns
Rise Time		t _R			56		ns
Turn-off Delay Time		t _{D(OFF)}			124		ns
Fall-Time		t _F			38		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				5	A
Maximum Body-Diode Pulsed Current		I _{SM}				20	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =5.0A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)		t _{rr}	I _S =5.0A, V _{GS} =0V,		308		nS
Reverse Recovery Charge		Q _{rr}	dl _F /dt =100A/μs		2.57		μC

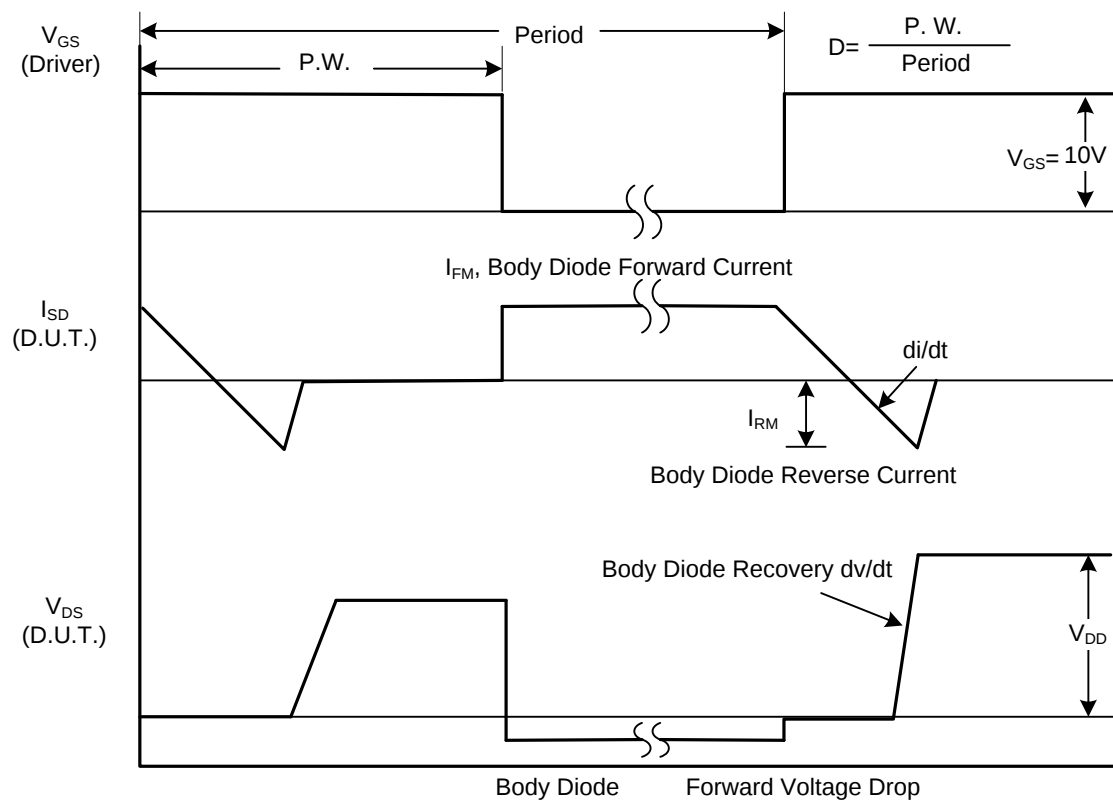
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

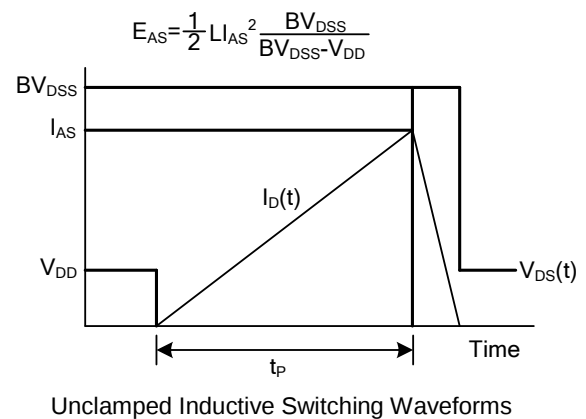
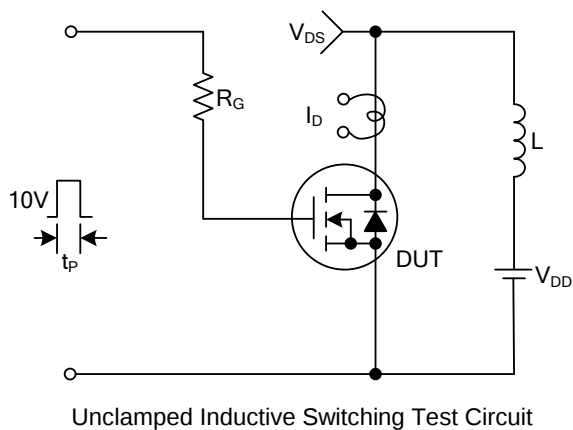
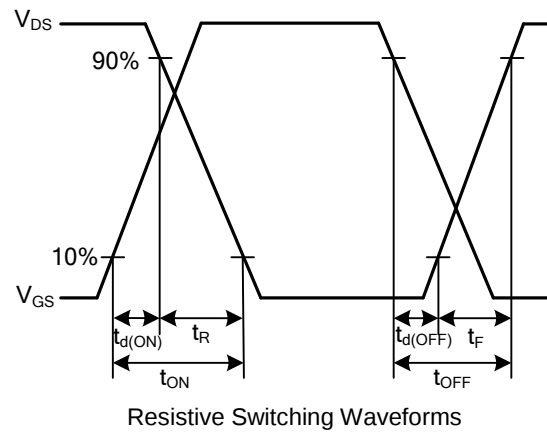
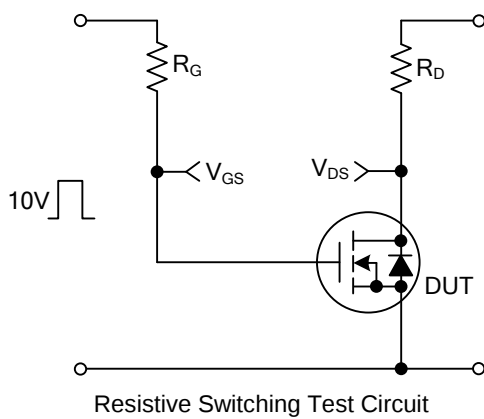
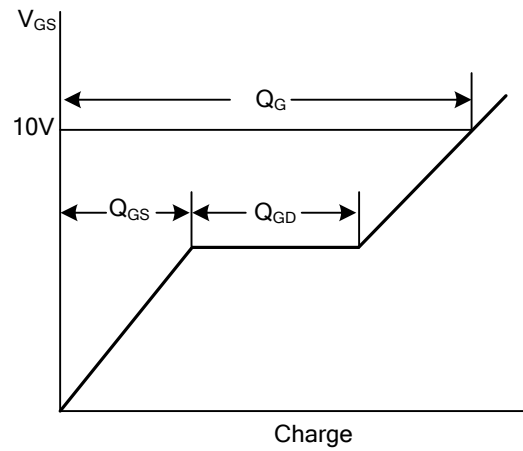
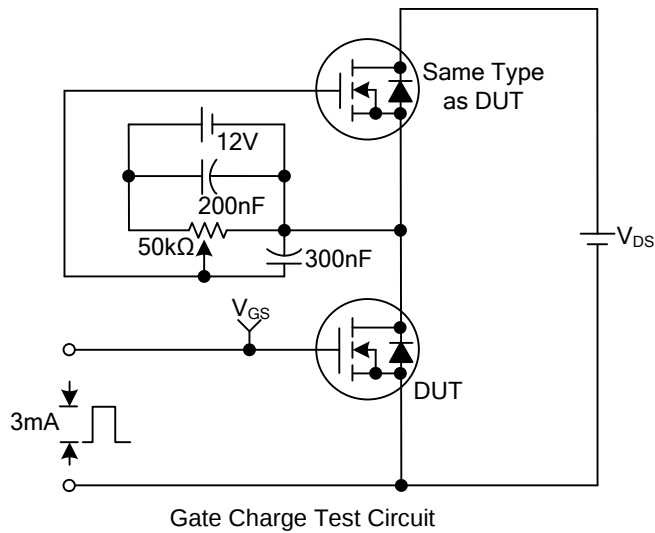


Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS



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