

PJQ4446P-AU

40V N-Channel Enhancement Mode MOSFET

Voltage

40 V

Current

48 A

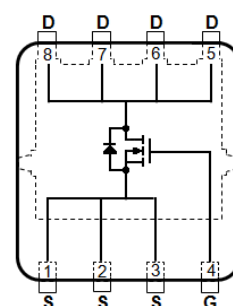
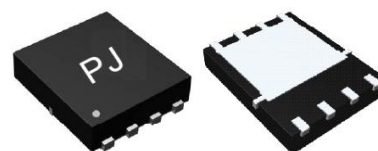
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@8A<9m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@4A<13m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultralow on-resistance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.001 ounces, 0.03 grams

DFN3333-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (Note 4)	$T_C=25^{\circ}C$	I_D	48	A
	$T_C=100^{\circ}C$		30	
Pulsed Drain Current (Note 1)	$T_C=25^{\circ}C$	I_{DM}	192	
Power Dissipation	$T_C=25^{\circ}C$	P_D	50	W
	$T_C=100^{\circ}C$		25	
Continuous Drain Current (Note 4)	$T_A=25^{\circ}C$	I_D	10.5	A
	$T_A=70^{\circ}C$		8.5	
Power Dissipation	$T_A=25^{\circ}C$	P_D	2.4	W
	$T_A=70^{\circ}C$		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^{\circ}C$
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	3	$^{\circ}C/W$
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature



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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	1.75	2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =8A	-	7.5	9	mΩ
		V _{GS} =4.5V, I _D =4A	-	10	13	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q _g	V _{DS} =20V, I _D =8A, V _{GS} =10V (Note 2,3)	-	22	-	nC
Gate-Source Charge	Q _{gs}		-	4.2	-	
Gate-Drain Charge	Q _{gd}		-	4.0	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHZ	-	1258	-	pF
Output Capacitance	C _{oss}		-	134	-	
Reverse Transfer Capacitance	C _{rss}		-	88	-	
Turn-On Delay Time	td _(on)	V _{DS} =15V, I _D =1A, V _{GS} =10V, R _G =3.3Ω (Note 2,3)	-	13	-	ns
Turn-On Rise Time	t _r		-	14	-	
Turn-Off Delay Time	td _(off)		-	45	-	
Turn-Off Fall Time	t _f		-	9	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	48	A
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V	-	0.7	1	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
4. The maximum current rating is package limited.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

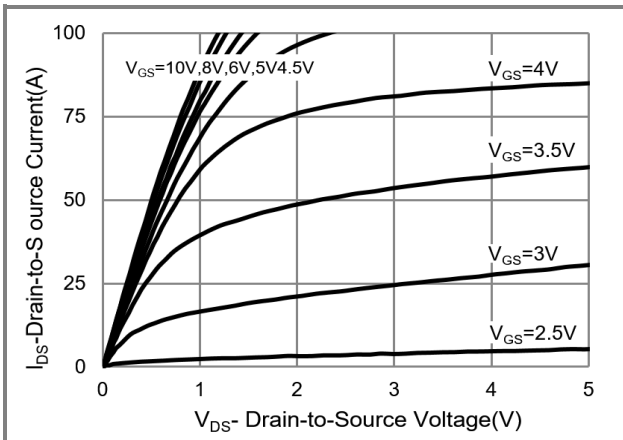


Fig.1 On-Region Characteristics

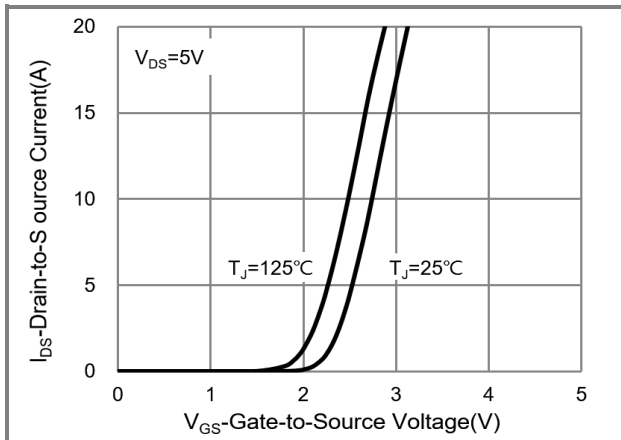


Fig.2 Transfer Characteristics

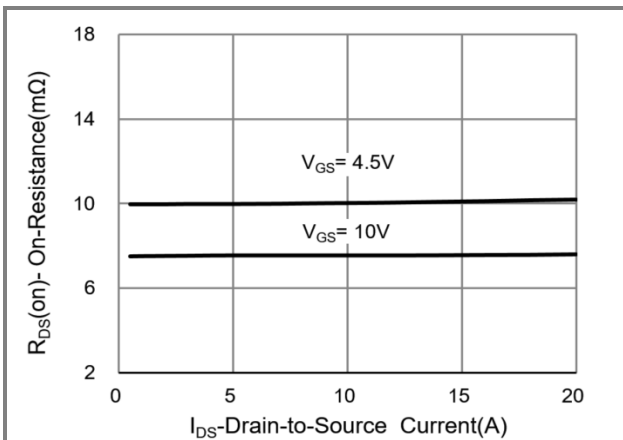


Fig.3 On-Resistance vs. Drain Current

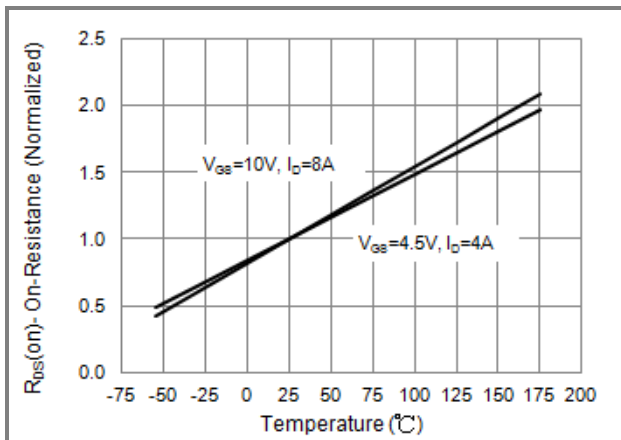


Fig.4 On-Resistance vs. Junction temperature

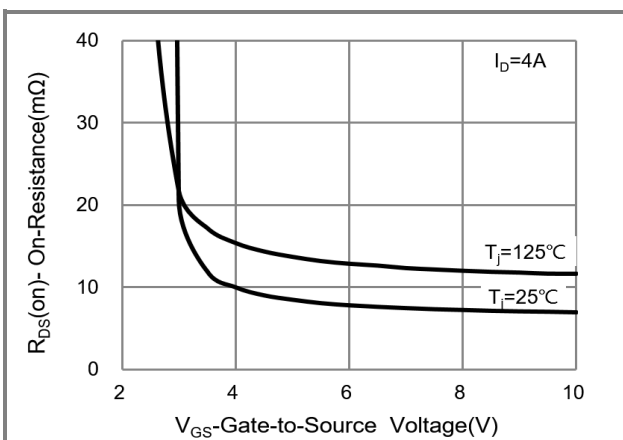


Fig.5 On-Resistance Variation with V_{GS}

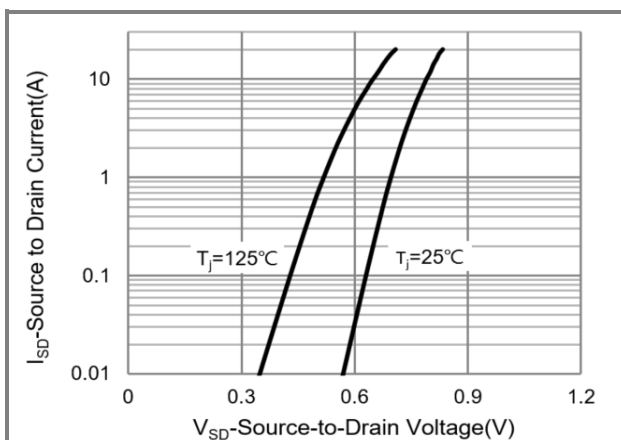
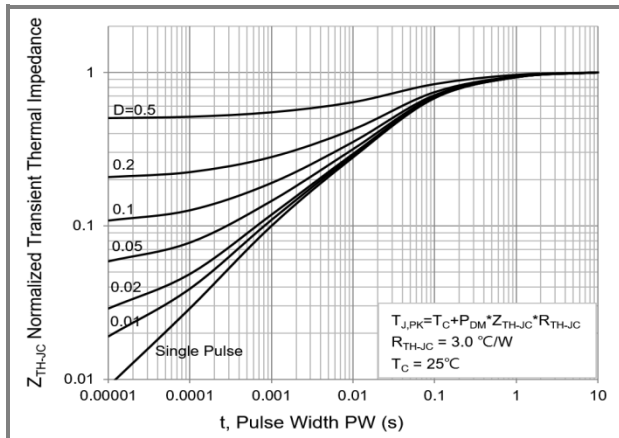
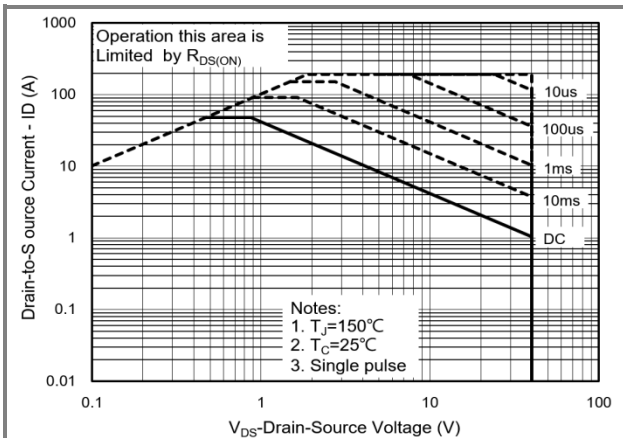
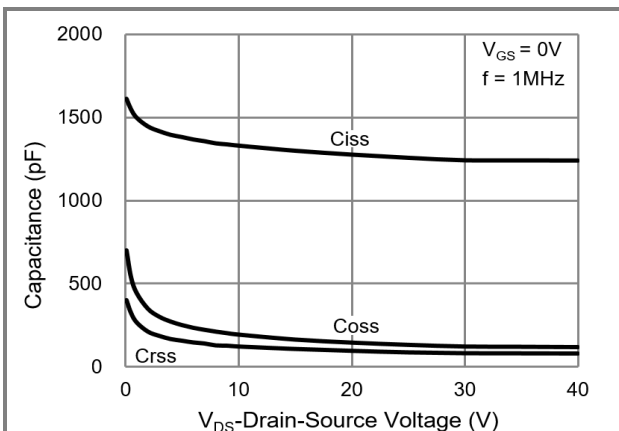
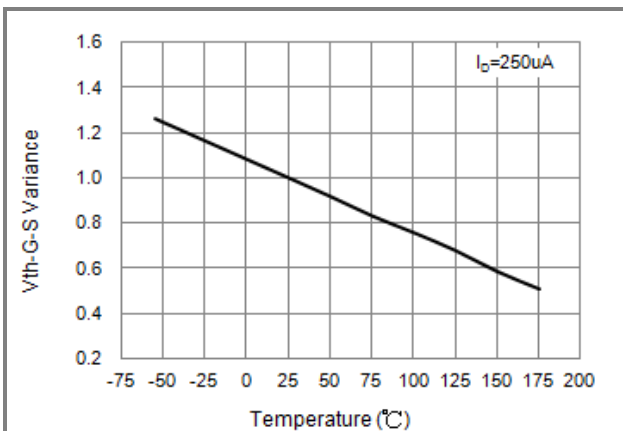
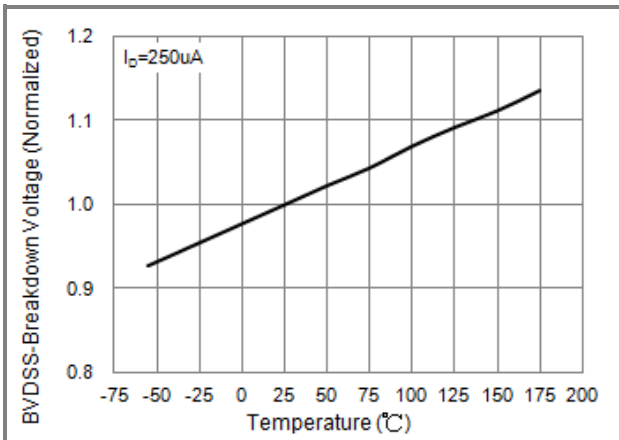
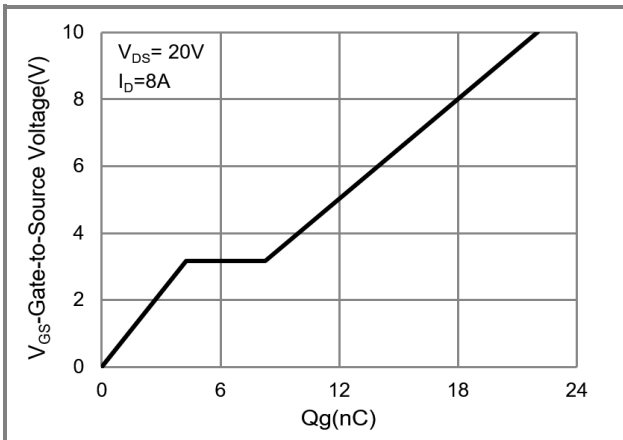


Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

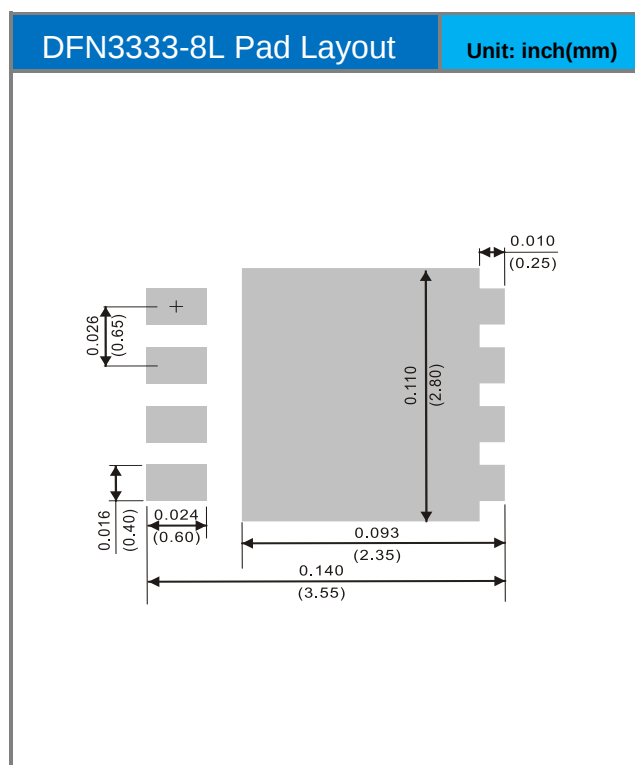
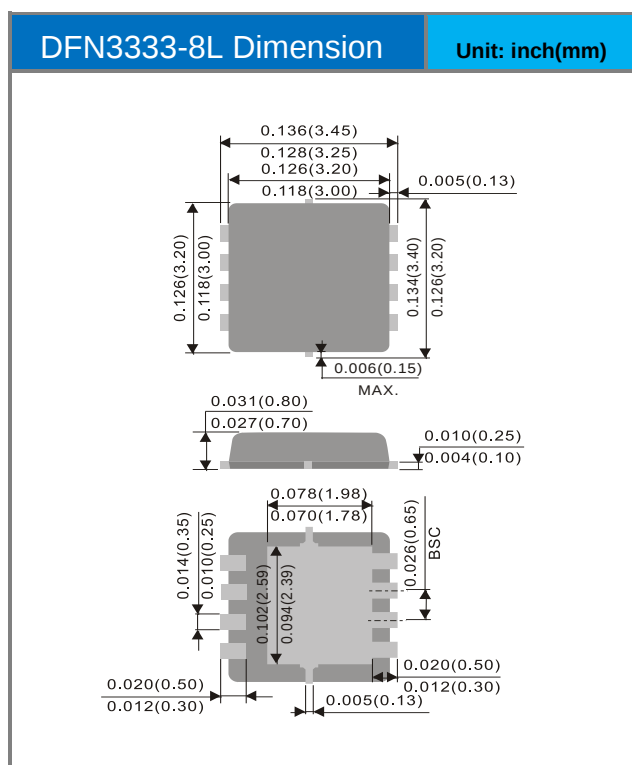


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Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJQ4446P-AU_R2_000A1	DFN3333-8L	5K pcs / 13" reel	4446	Halogen free

Packaging Information & Mounting Pad Layout





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